

FIG. 1A

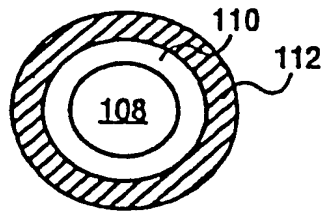


FIG. 1B

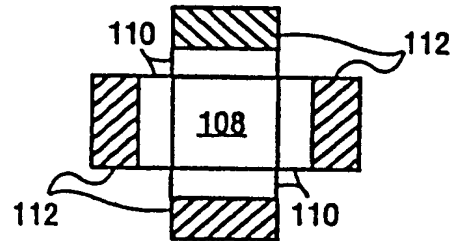


FIG. 1C

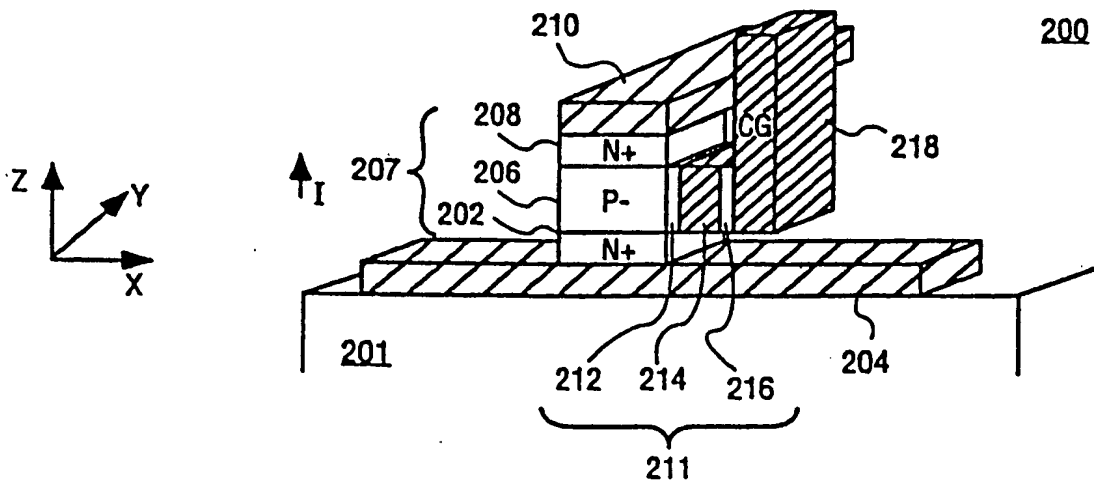
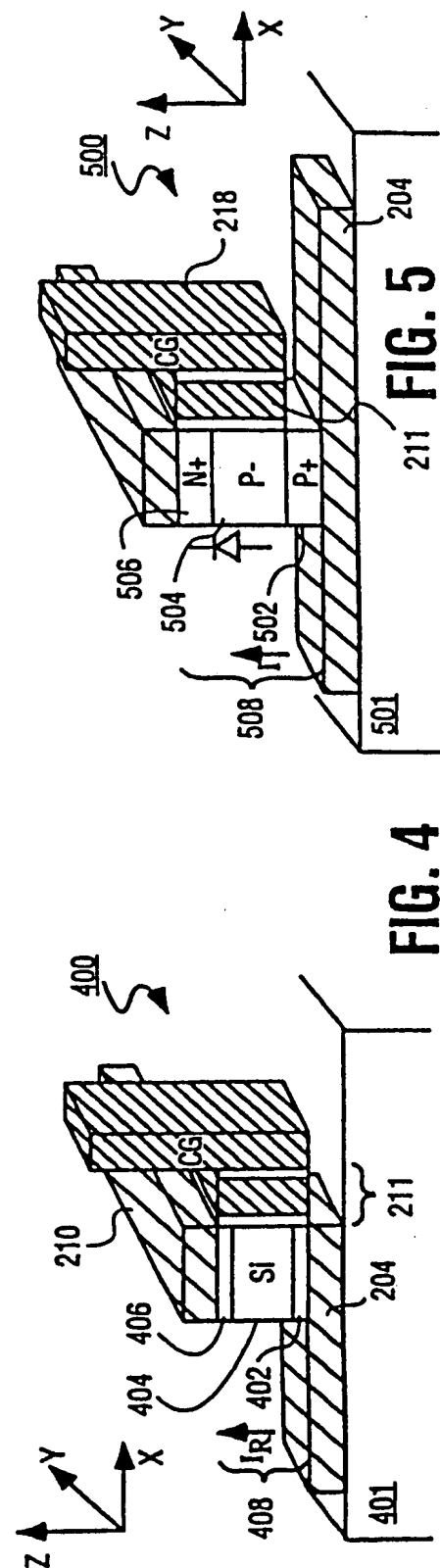
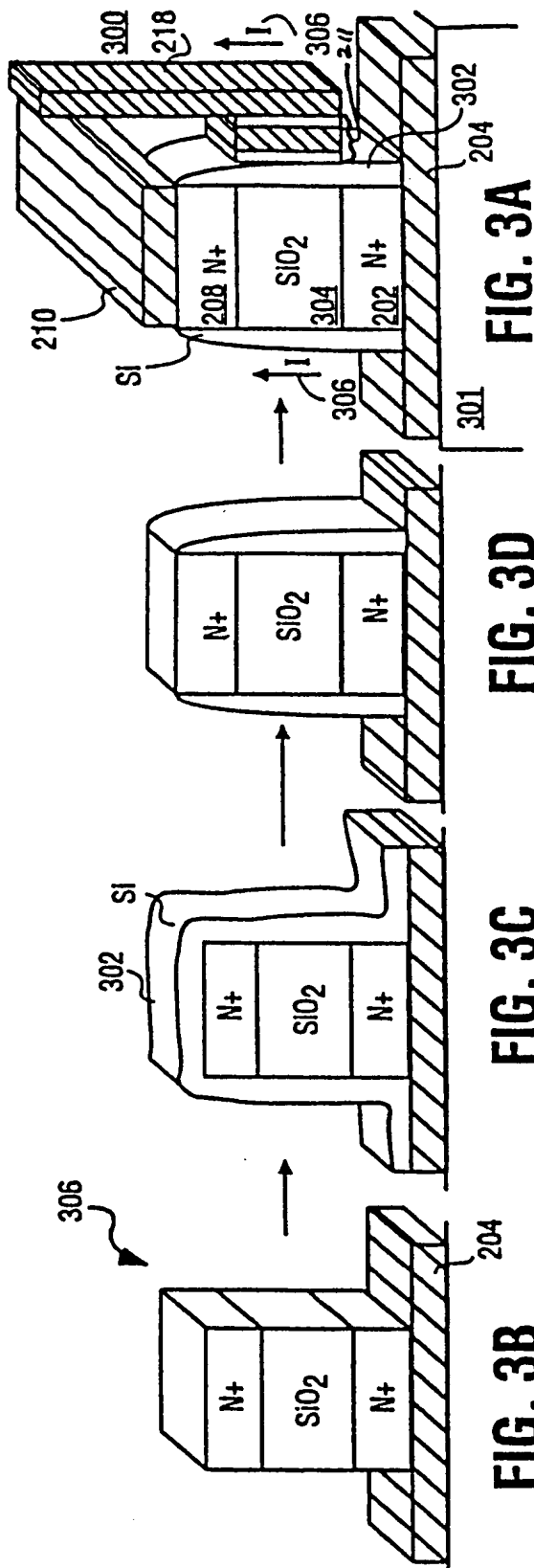


FIG. 2



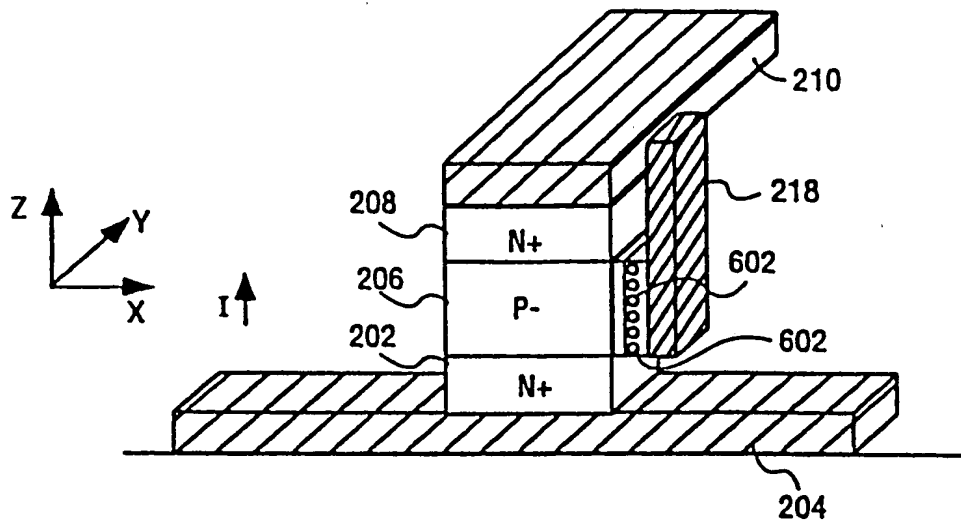


FIG. 6

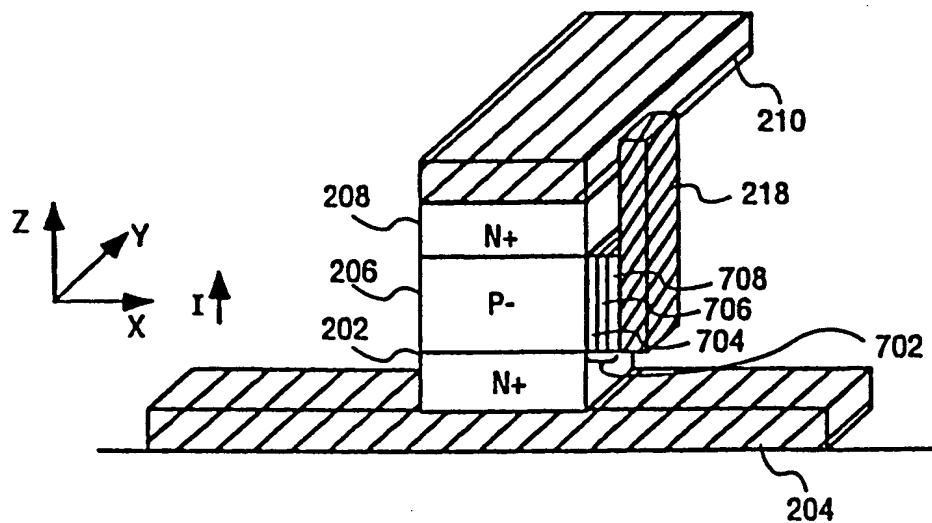


FIG. 7

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FIG. 8A

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DEVICES AND METHODS FOR MAKING SAME

Inventor(s): Thomas H. LEE et al.

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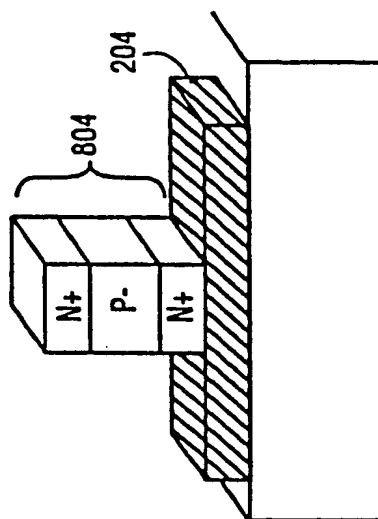
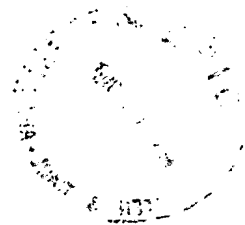


FIG. 8B

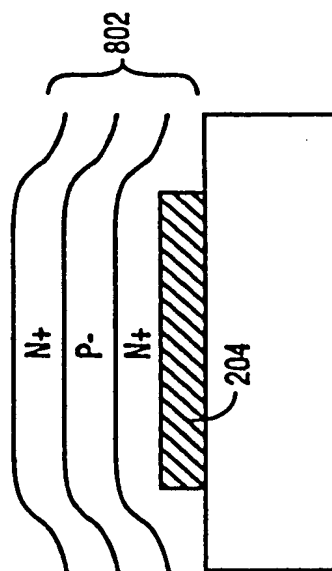


FIG. 8A

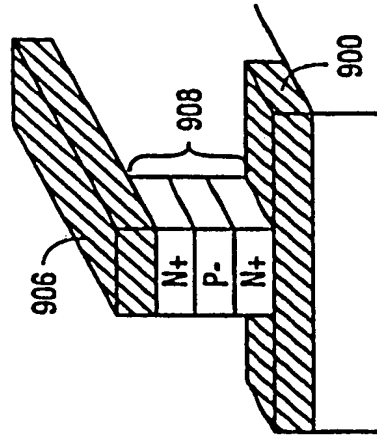


FIG. 9B

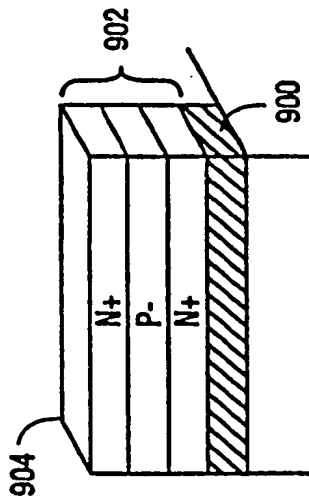


FIG. 9A

104711 3492660

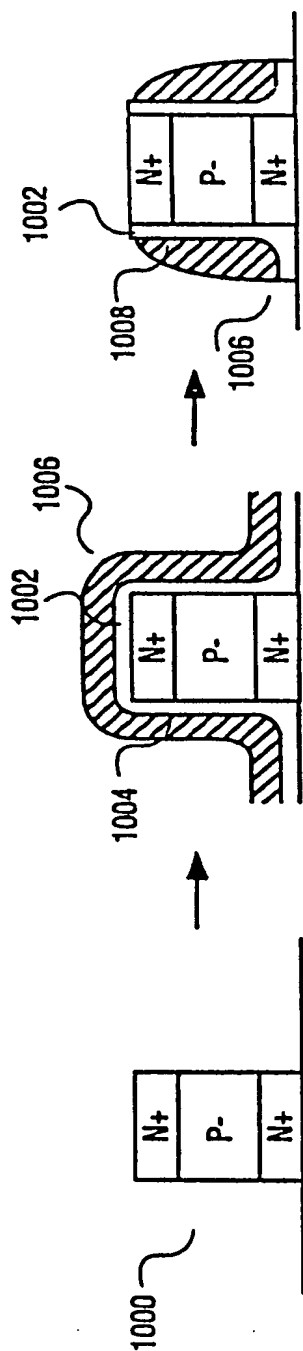


FIG. 10A

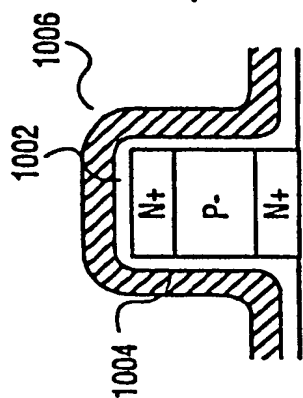


FIG. 10B

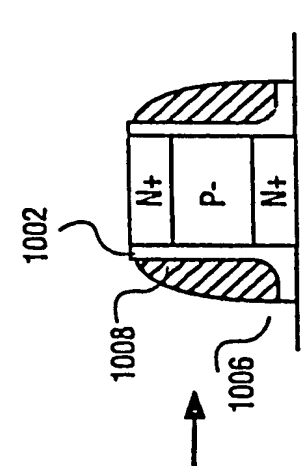


FIG. 10C

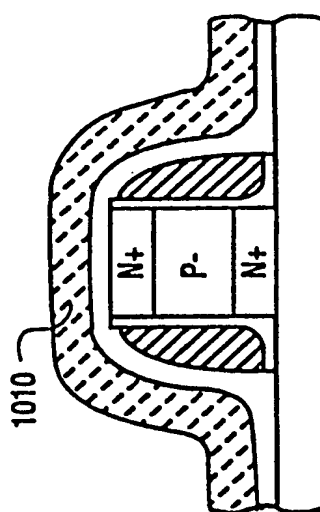


FIG. 10D

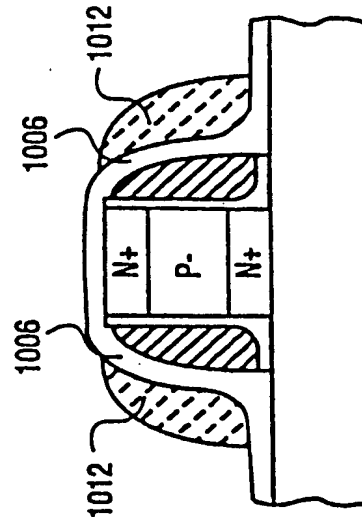


FIG. 10E

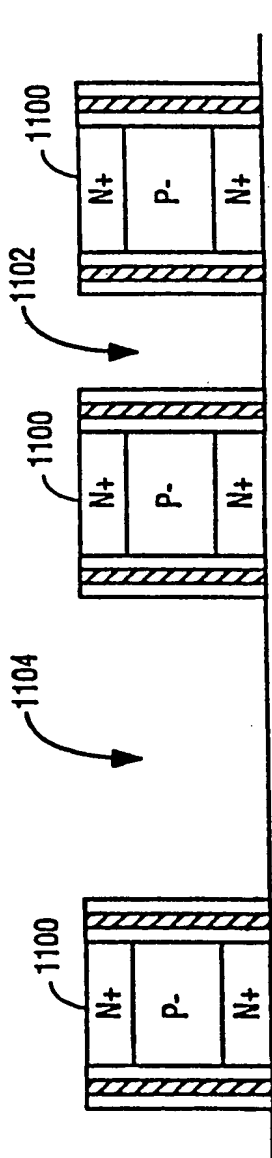


FIG. 11A

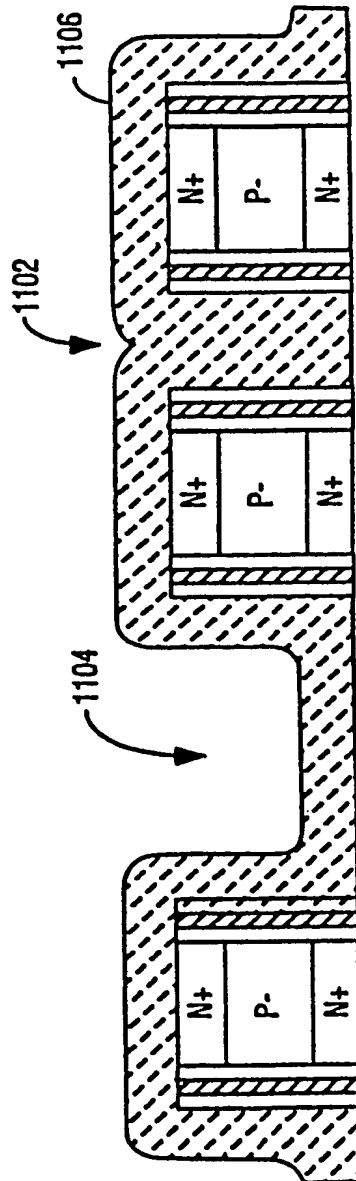


FIG. 11B

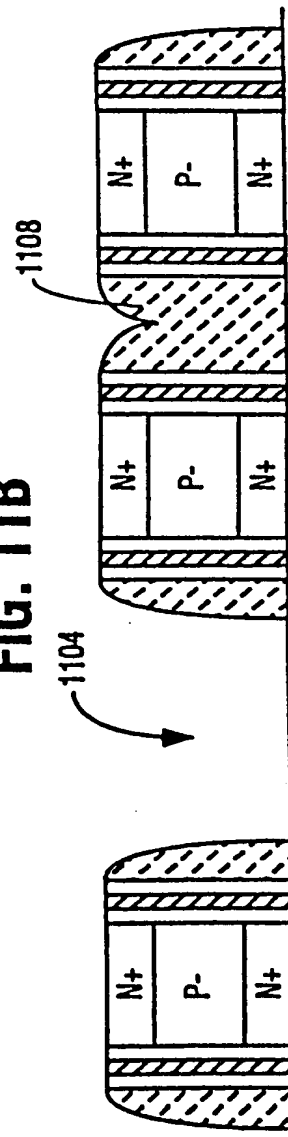


FIG. 11C

FIG. 11A

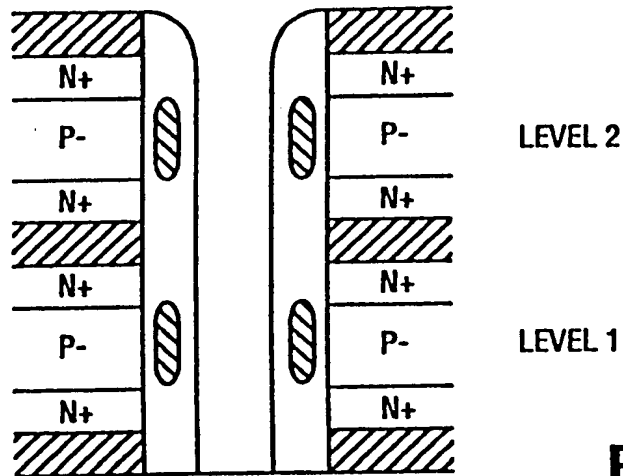


FIG. 12A

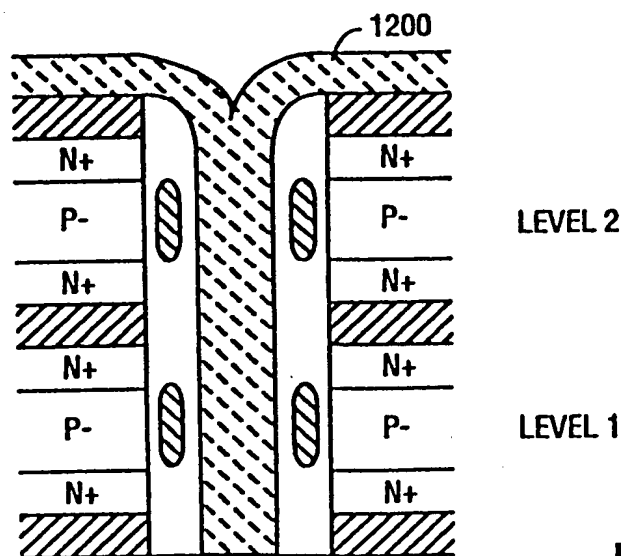


FIG. 12B

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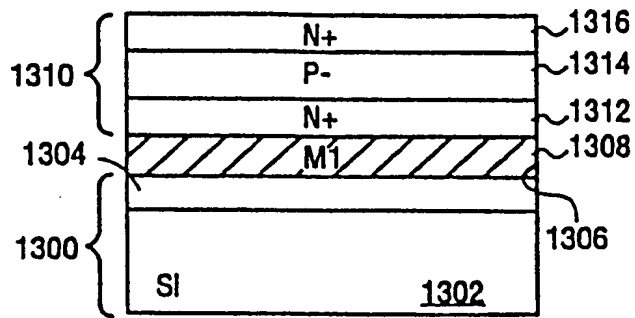


FIG. 13A

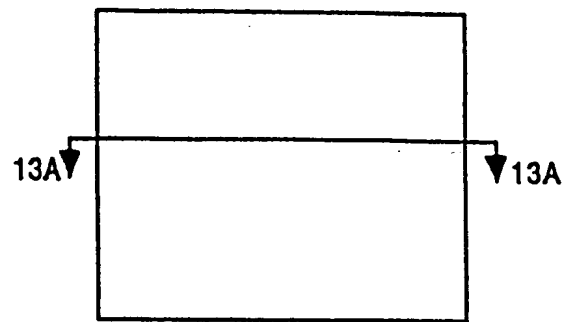


FIG. 13B

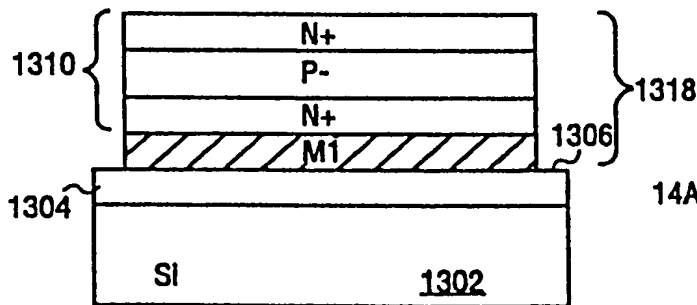


FIG. 14A

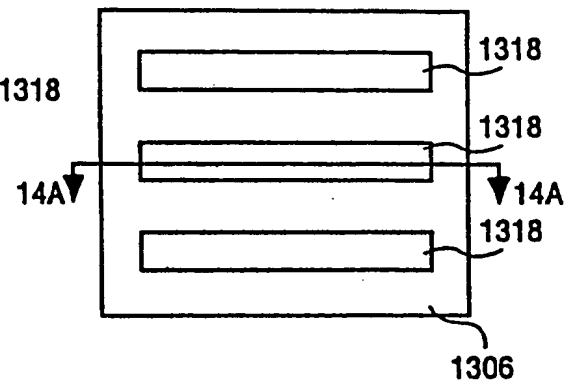


FIG. 14B

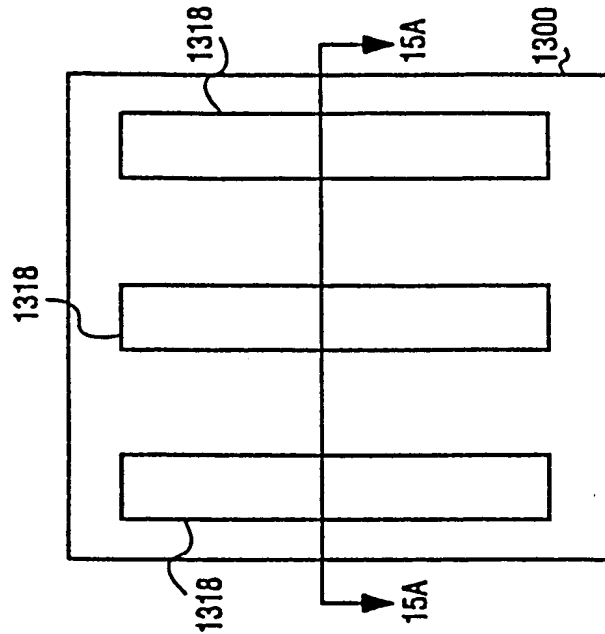


FIG. 15B

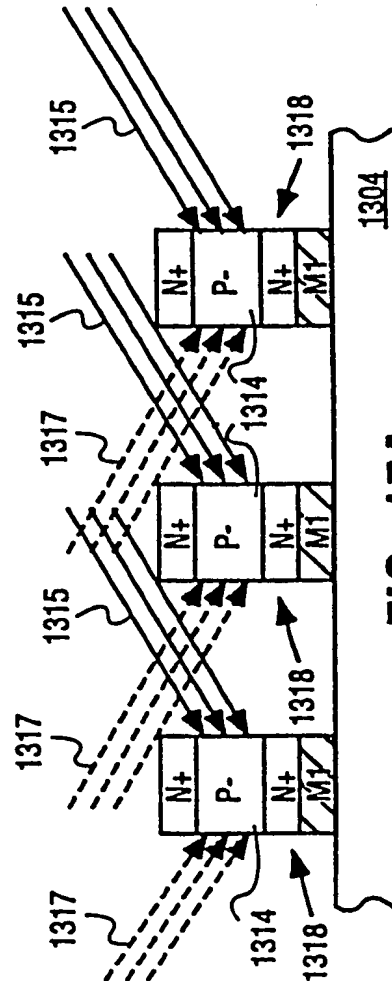


FIG. 15A

FIG. 15A

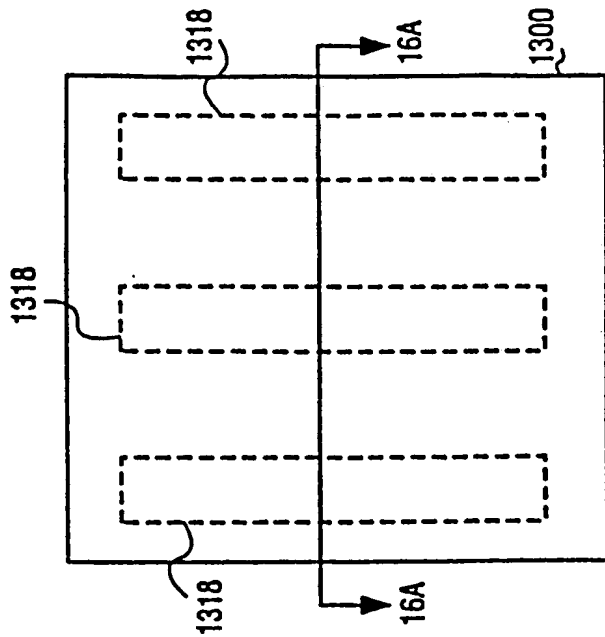


FIG. 16B

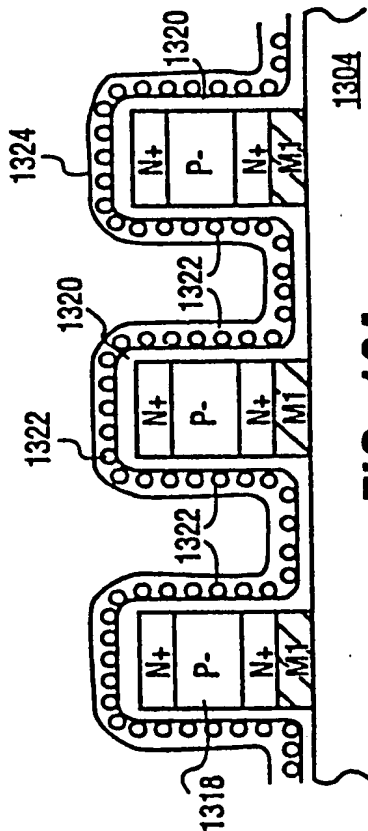


FIG. 16A

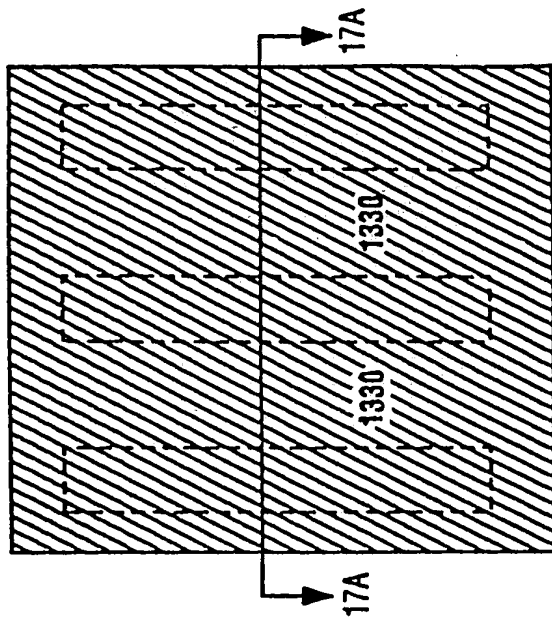


FIG. 17B

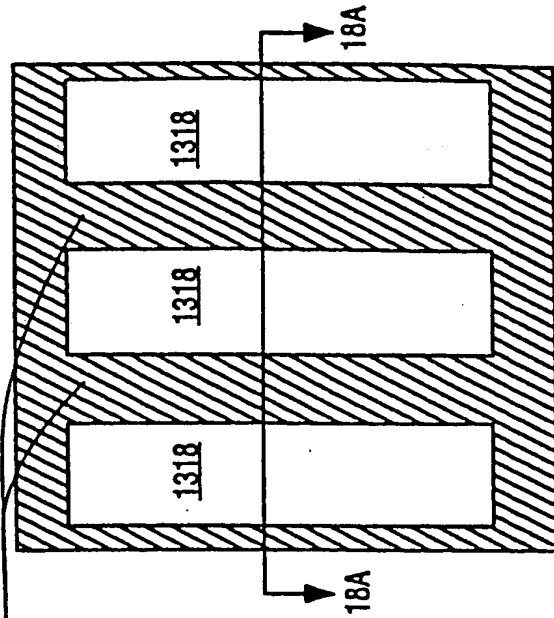


FIG. 18B

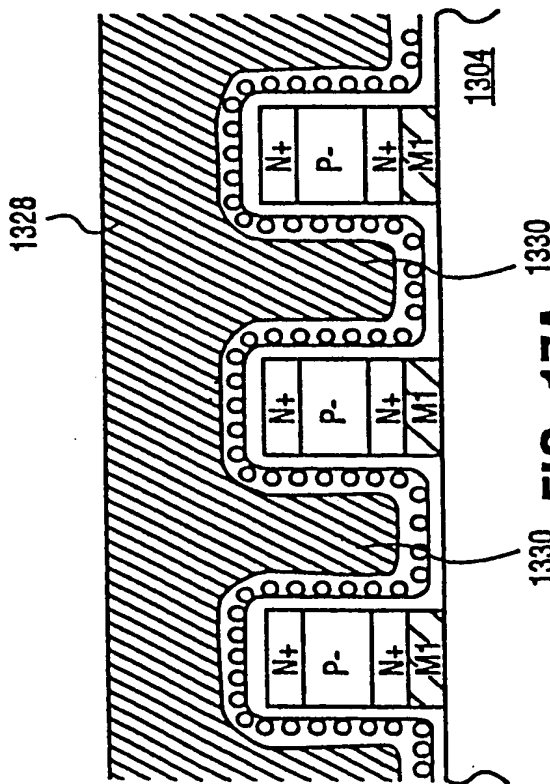


FIG. 17A

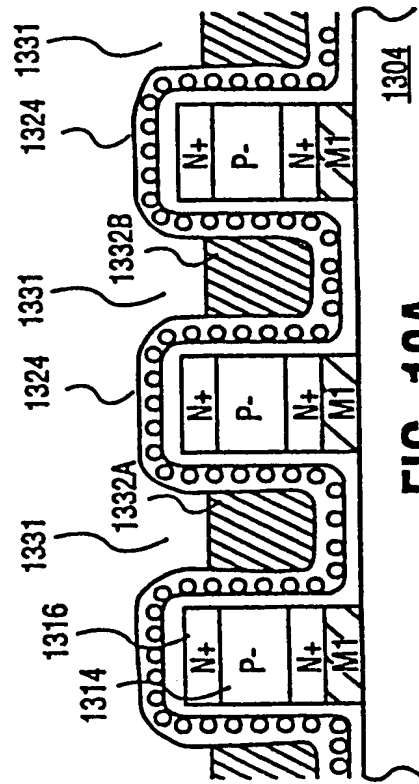


FIG. 18A

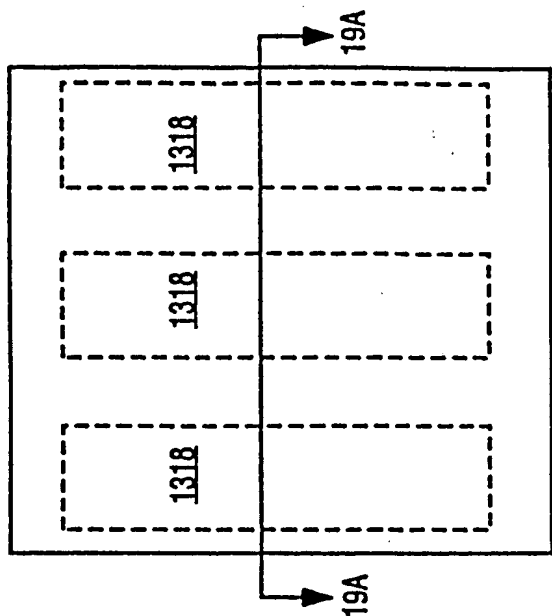


FIG. 19B

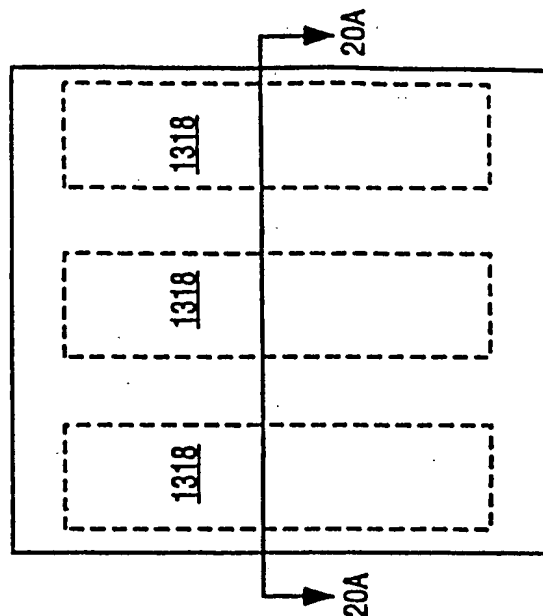


FIG. 20B

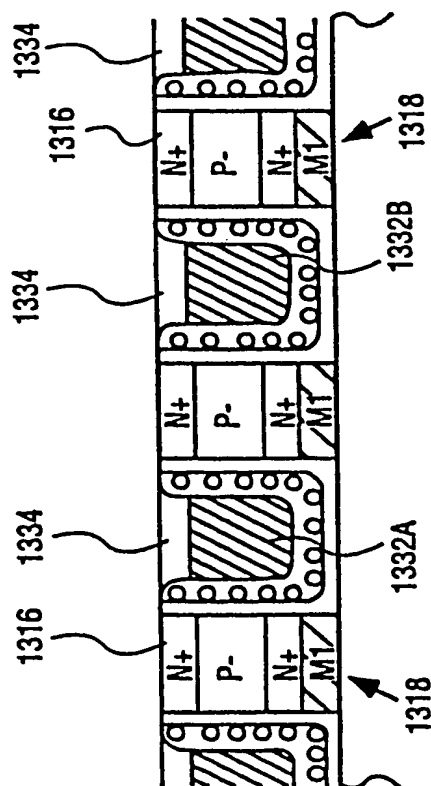


FIG. 19A

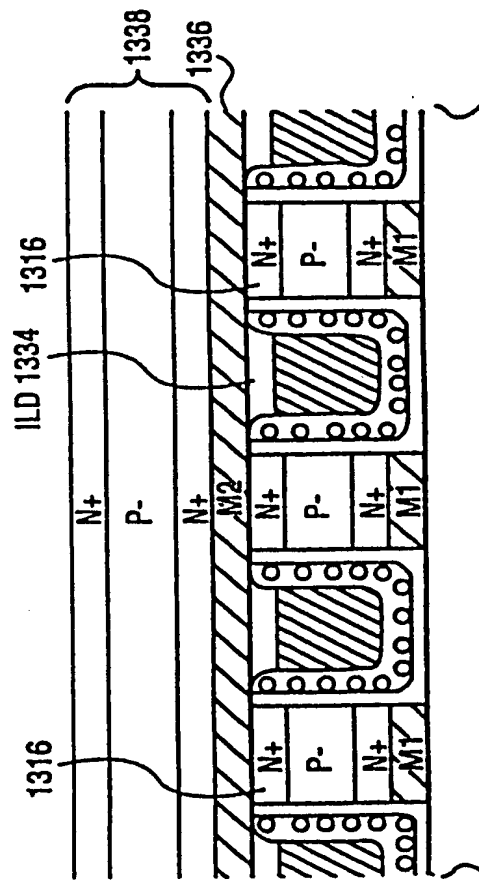


FIG. 20A

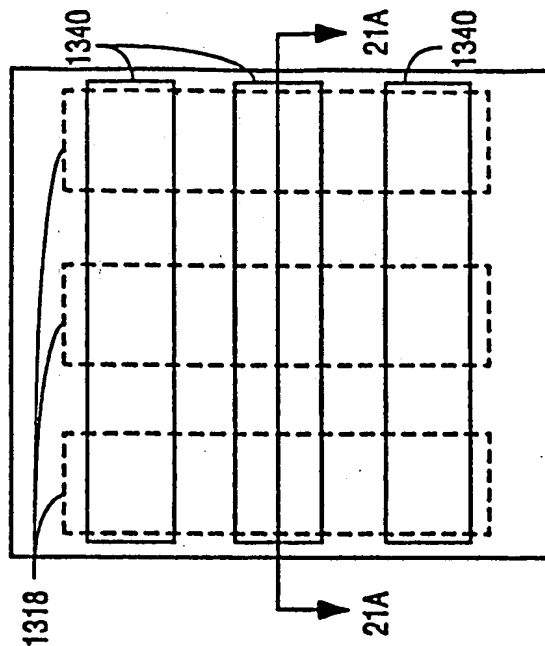


FIG. 21B

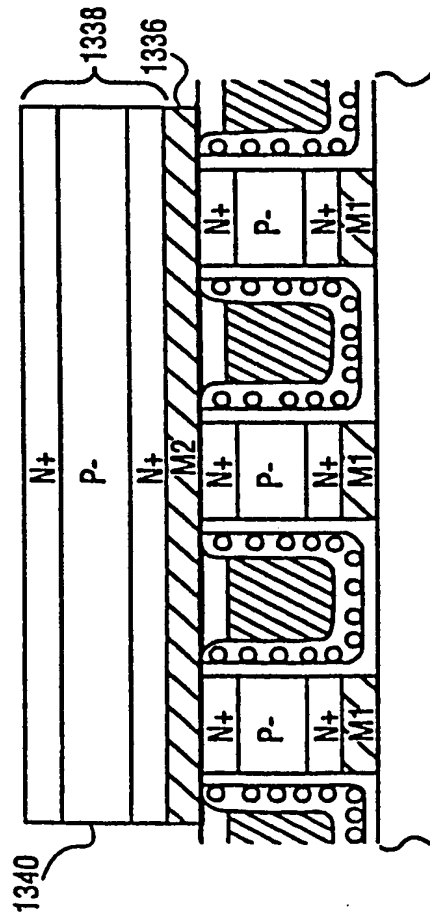


FIG. 21A

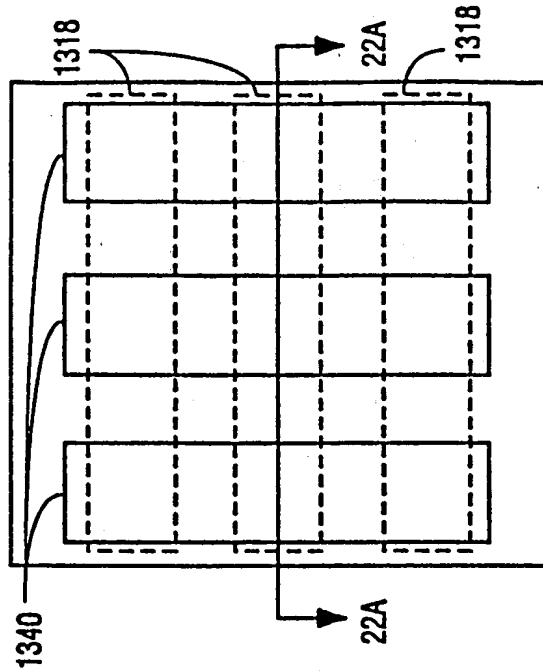


FIG. 22B

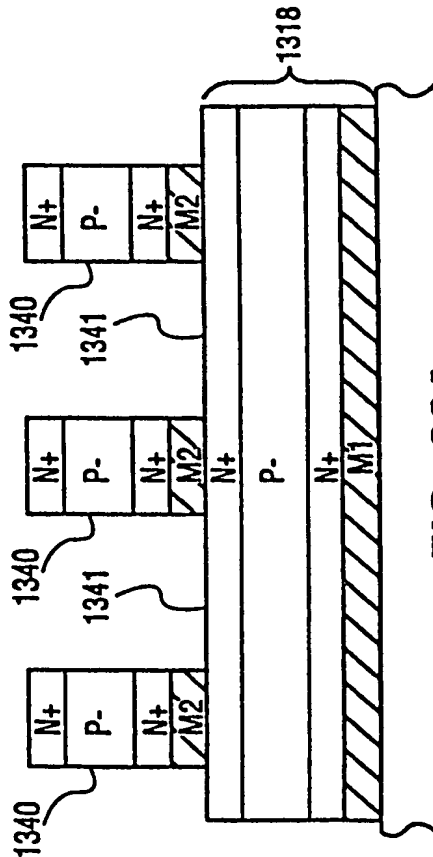


FIG. 22A

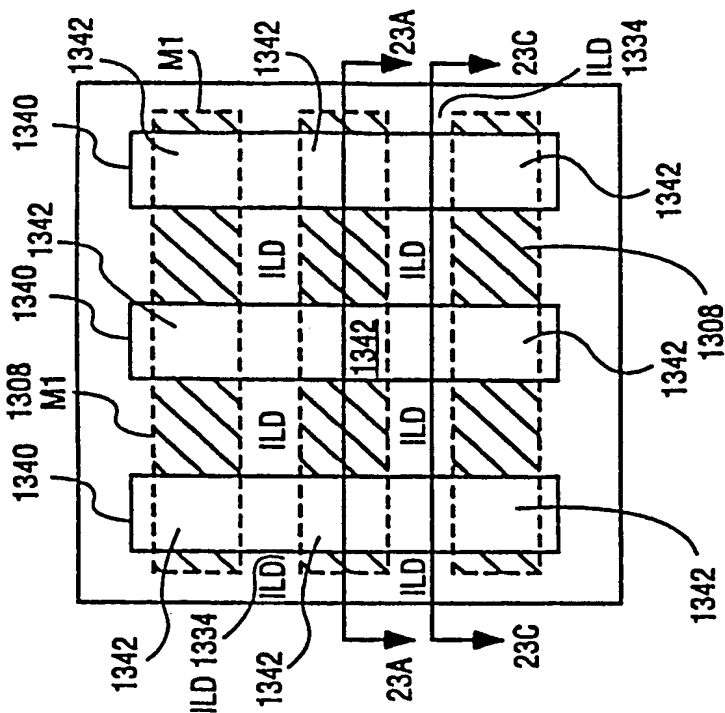


FIG. 23B

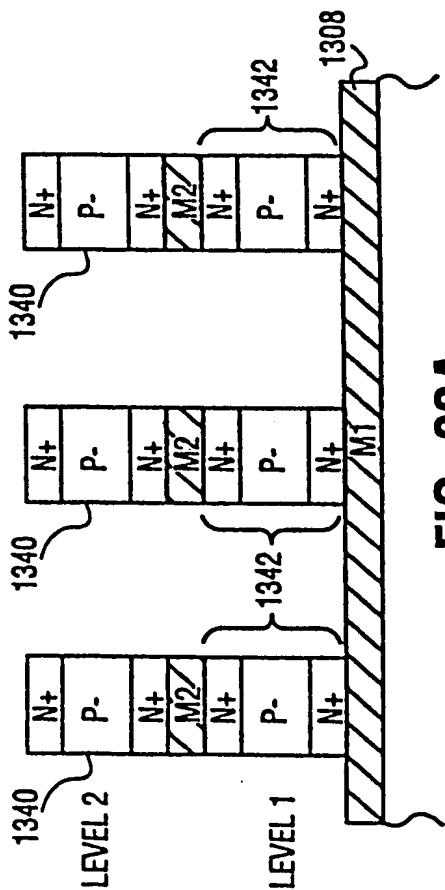


FIG. 23A

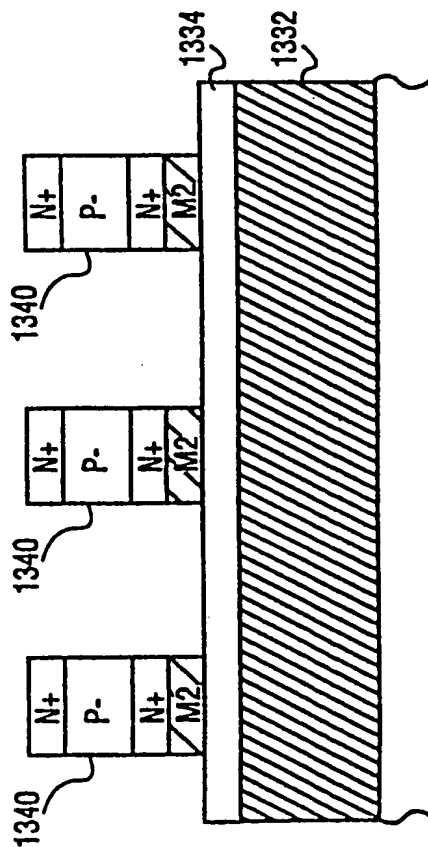


FIG. 23C



FIG. 24

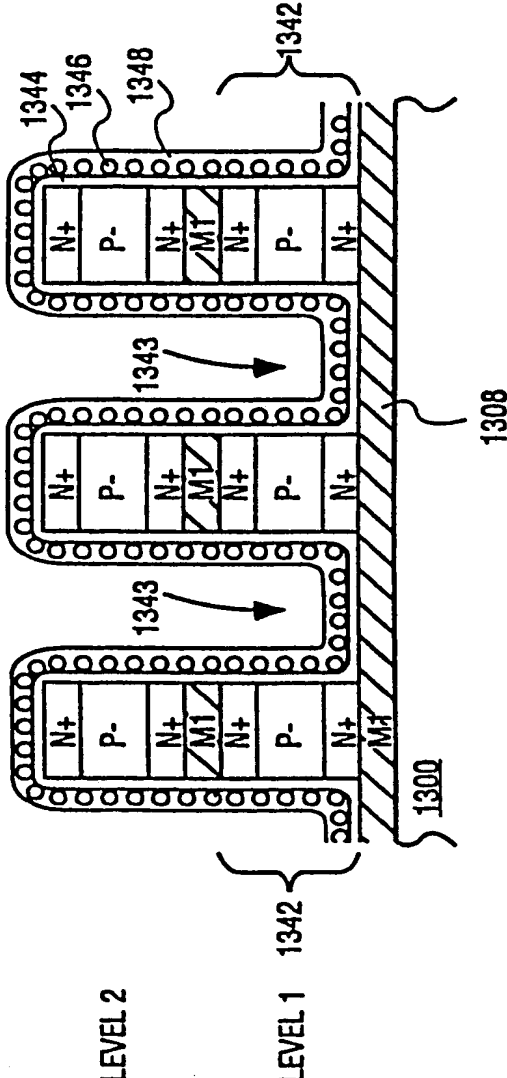


FIG. 24

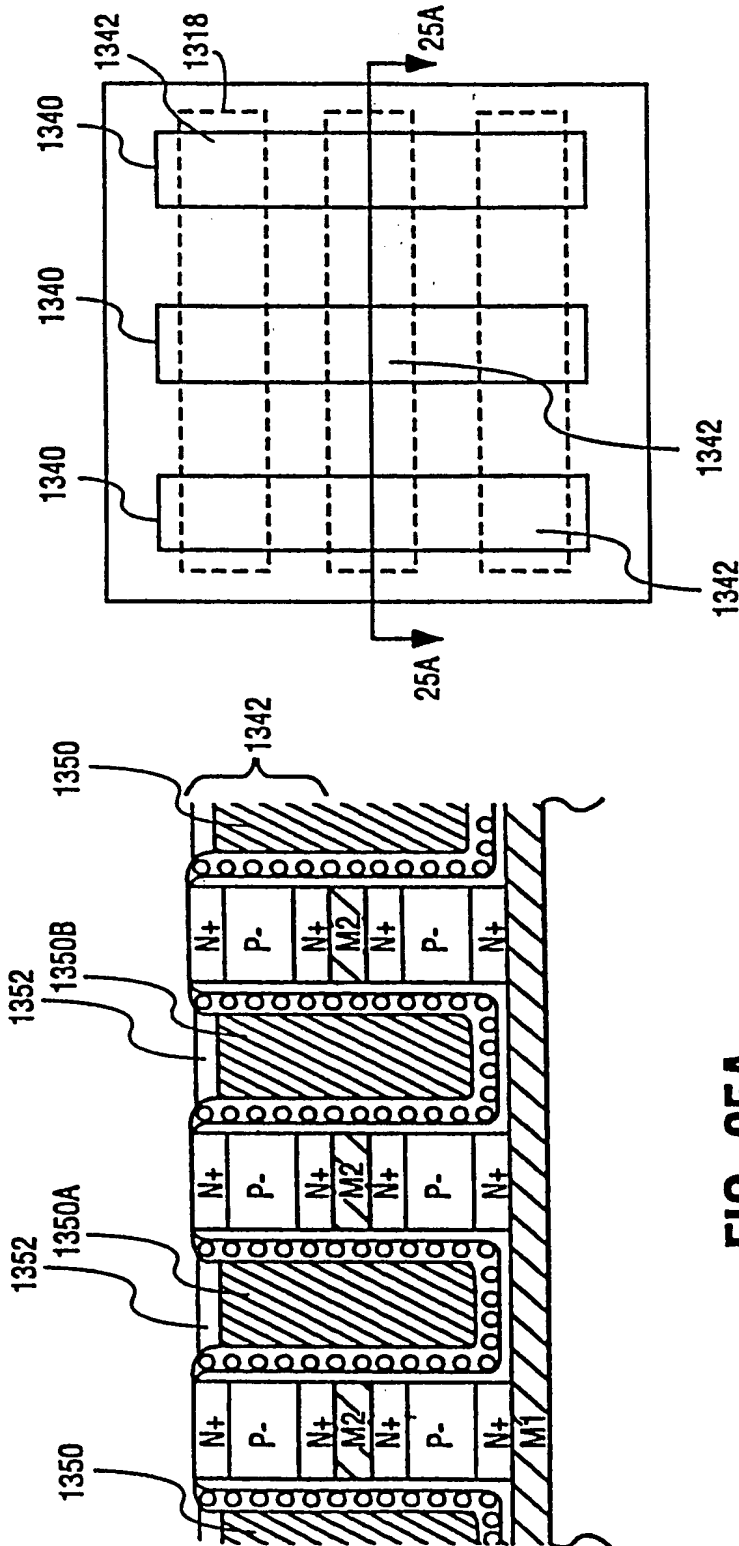


FIG. 25A

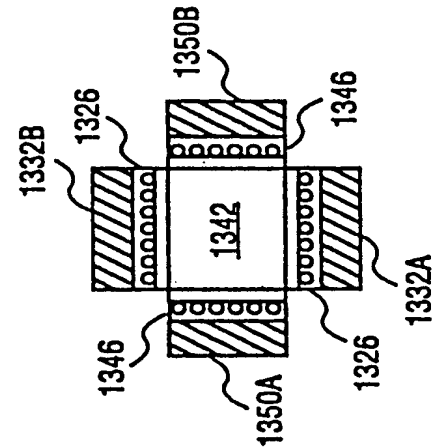


FIG. 26

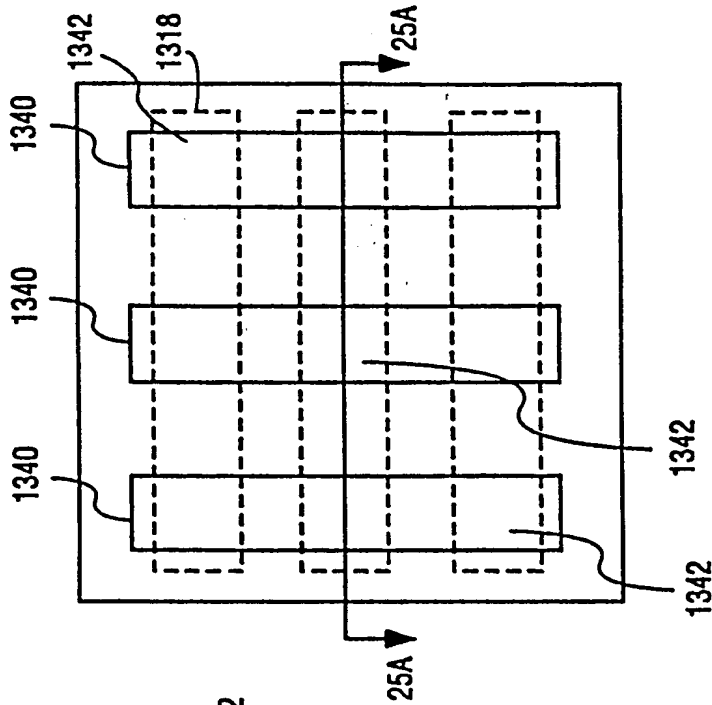


FIG. 25B

FIG. 27A

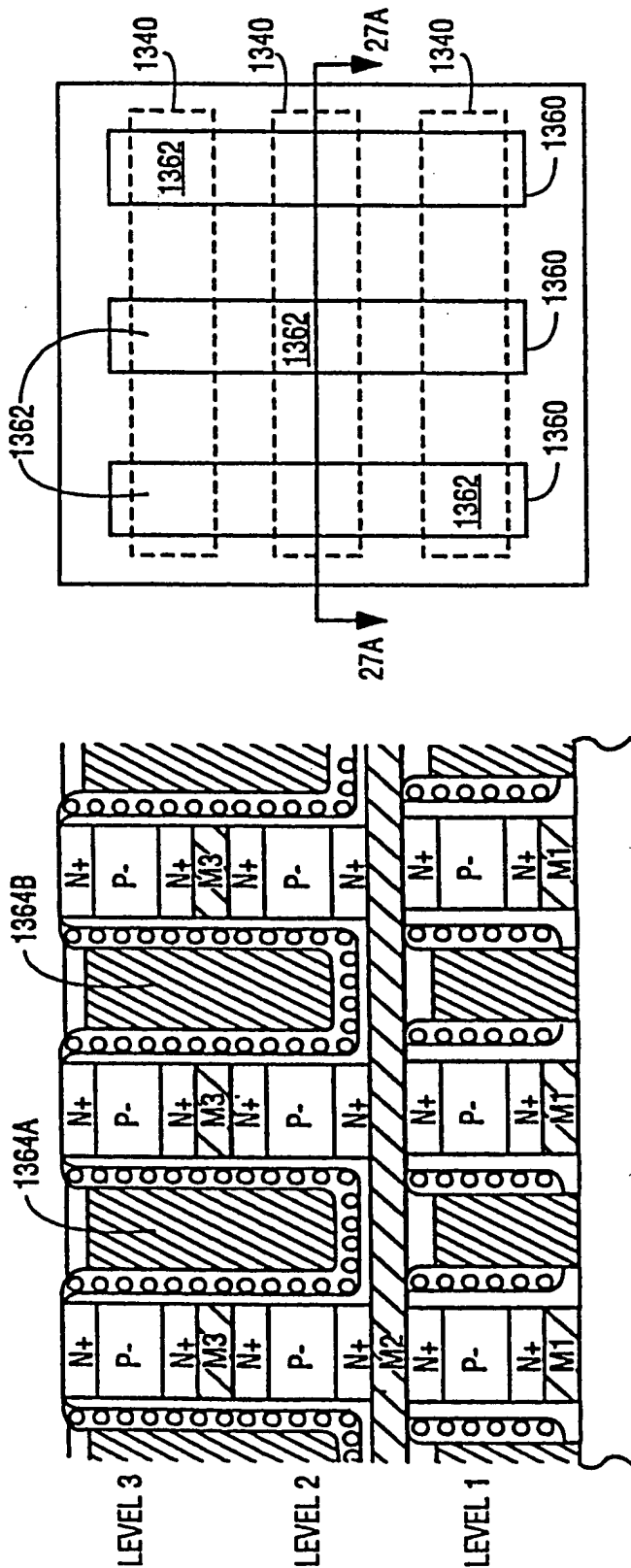


FIG. 27B

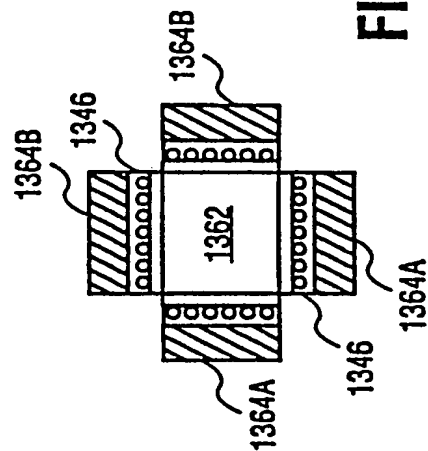


FIG. 28



FIG. 29A

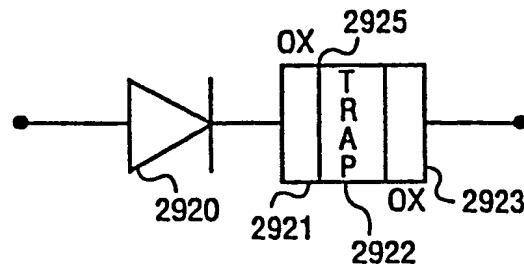
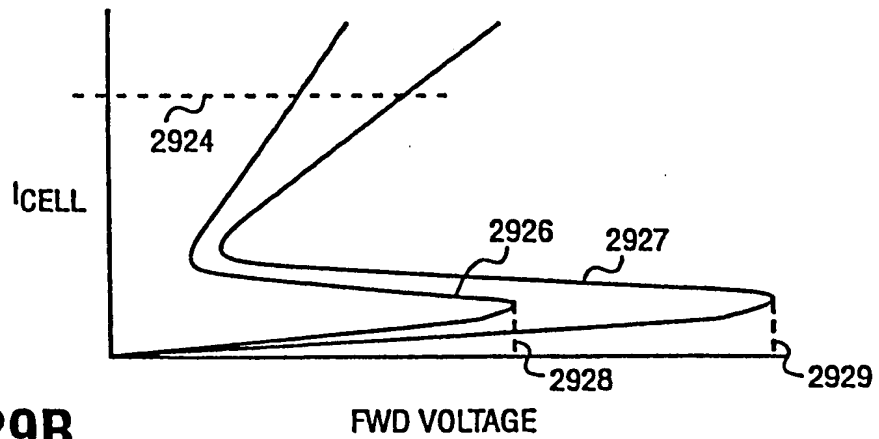


FIG. 29B



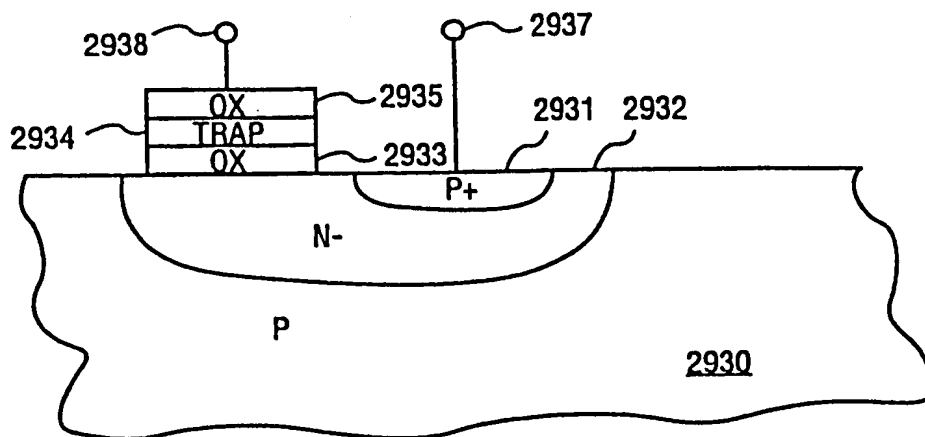


FIG. 30

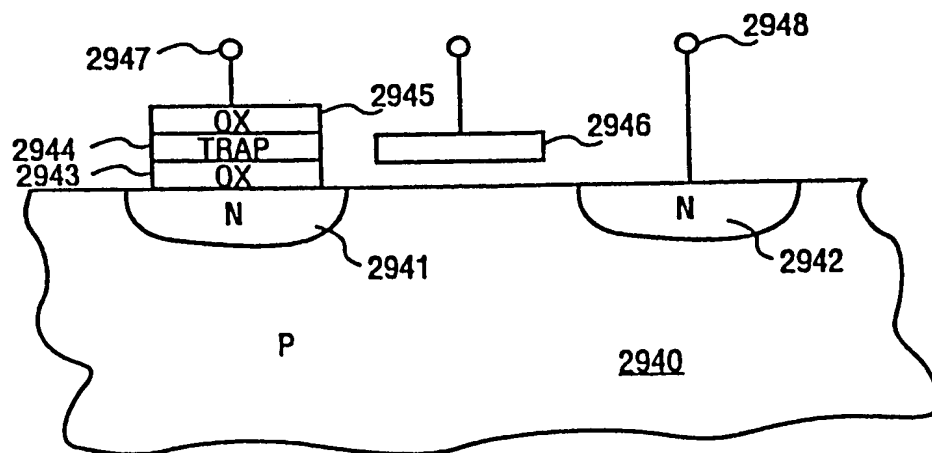
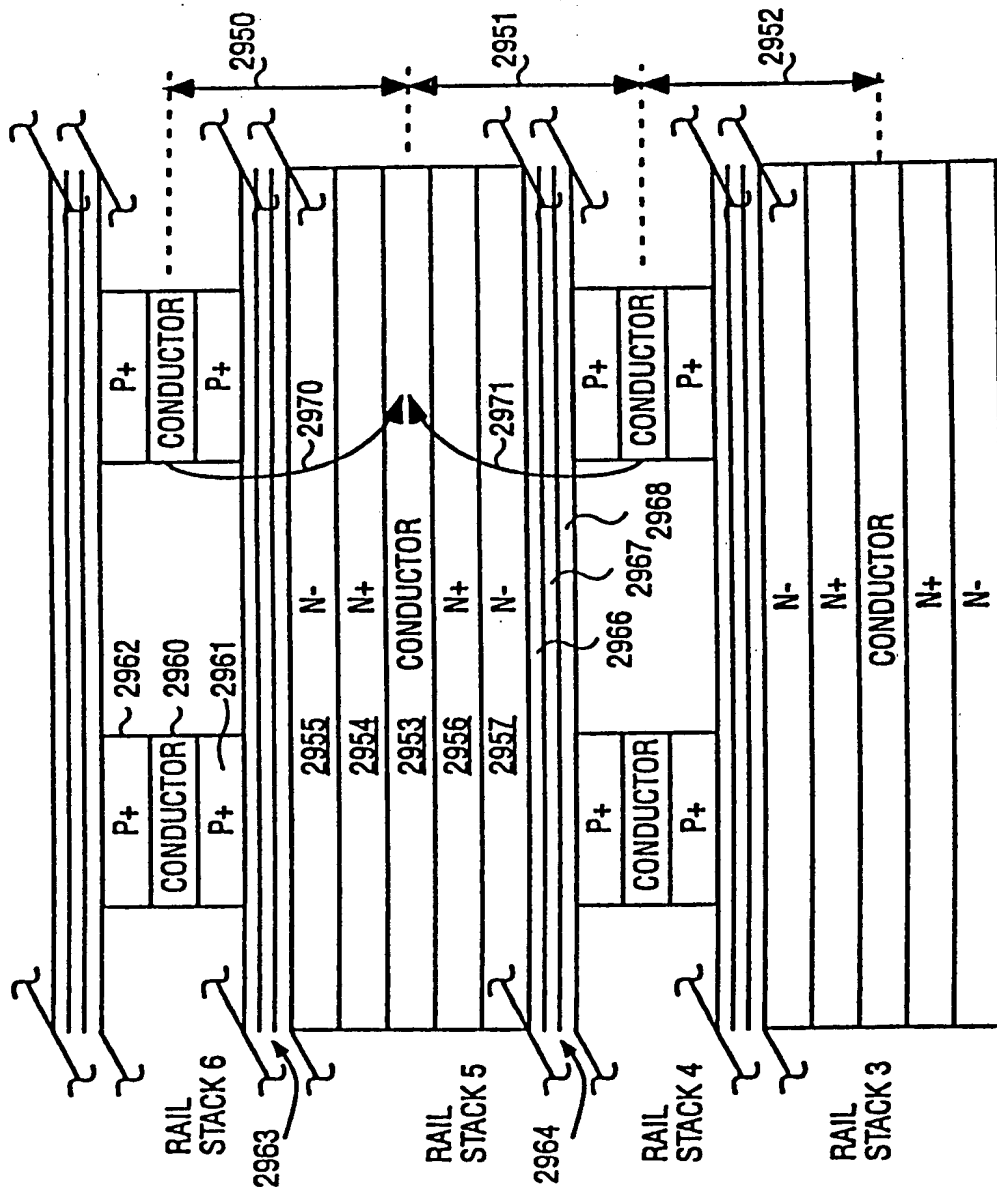


FIG. 31

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FIG. 32



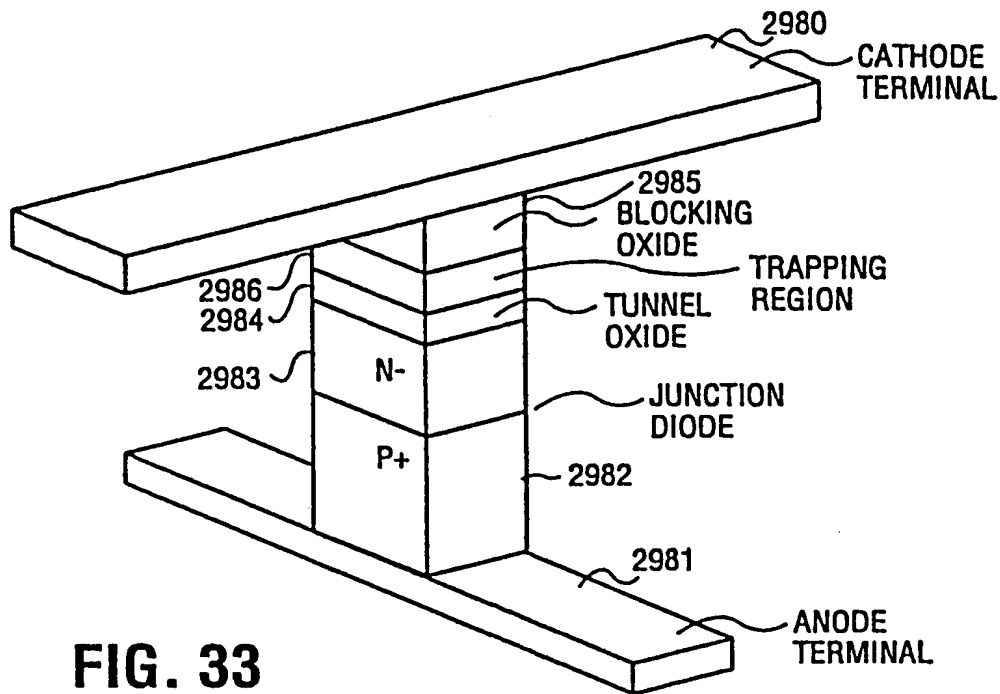
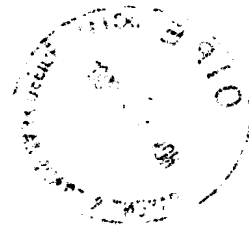


FIG. 33

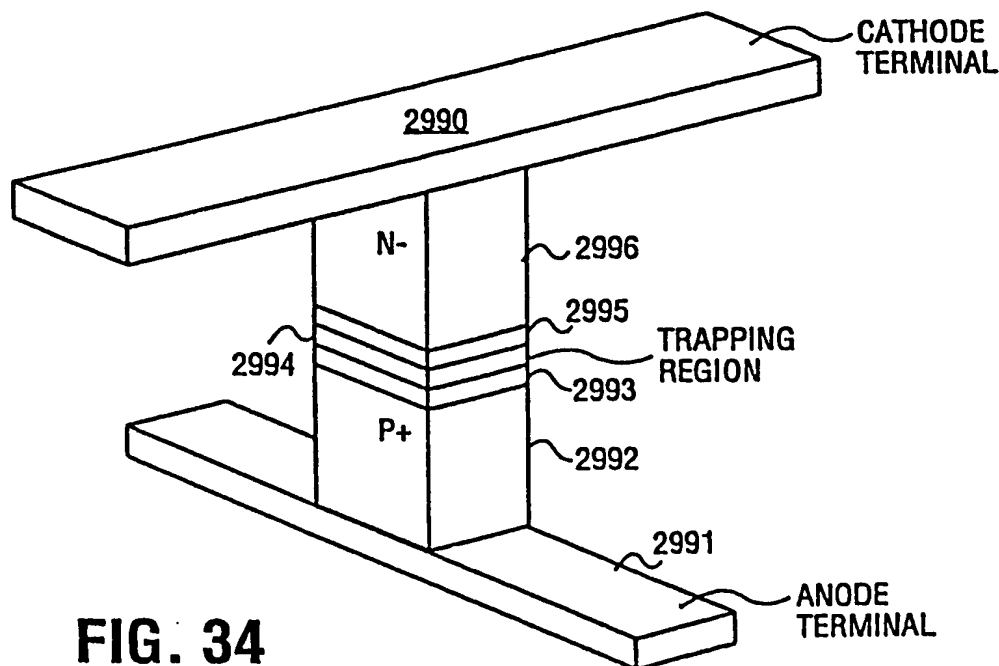


FIG. 34

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FIG. 35

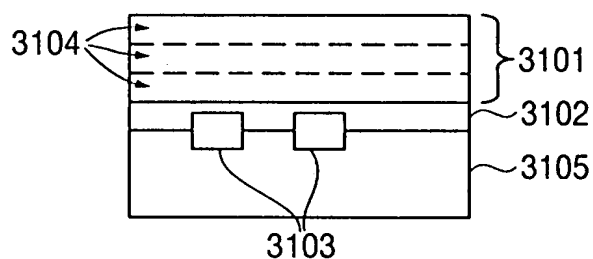


FIG. 36

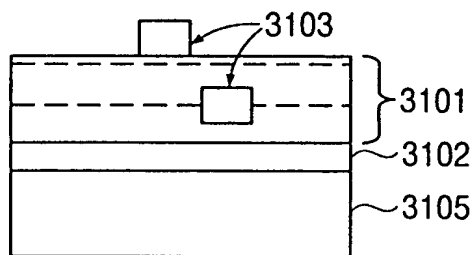




FIG. 37

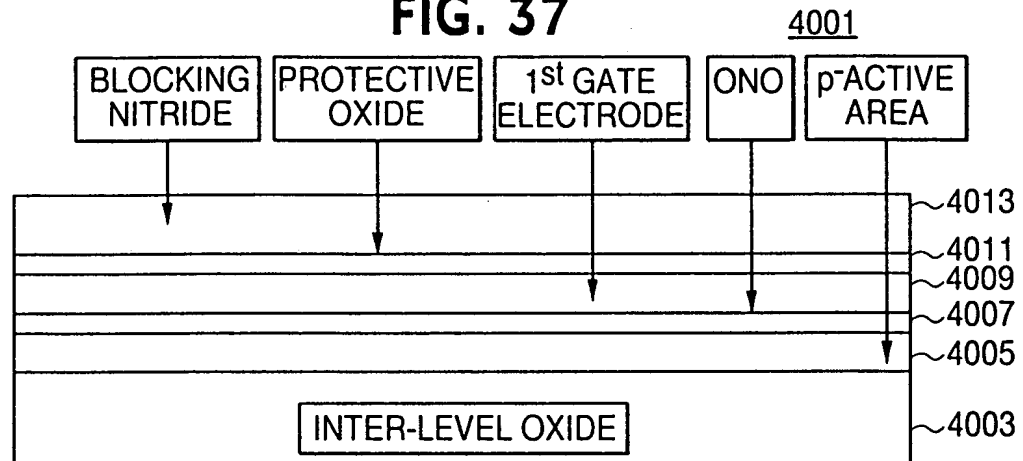
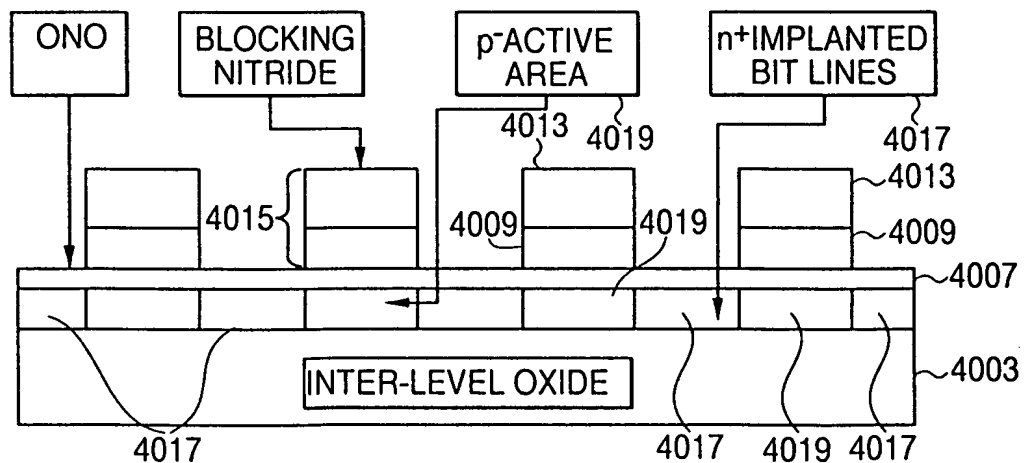
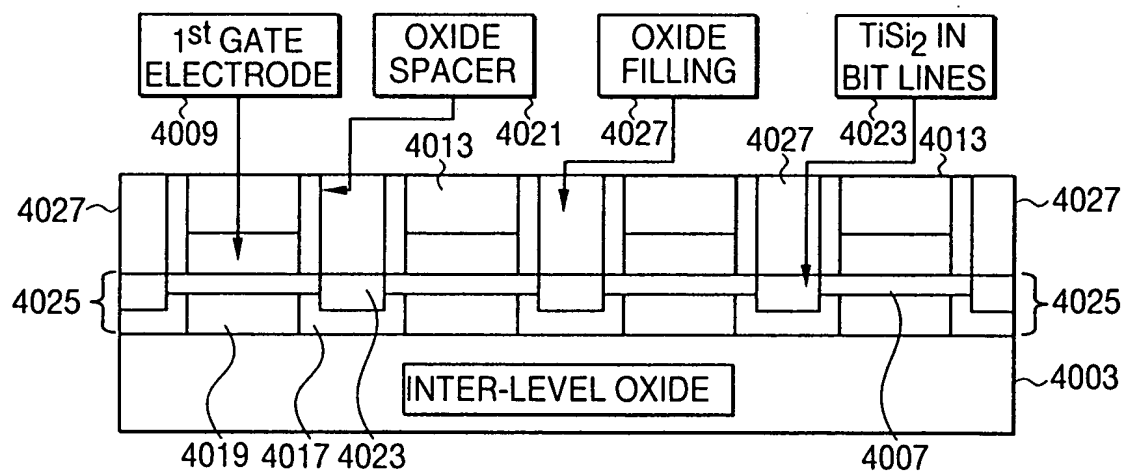


FIG. 38





1st GATE ELECTRODE 4009

OXIDE SPACER 4021

OXIDE FILLING 4027

TiSi₂ IN BIT LINES 4023

4029

4021

4027

4025

INTER-LEVEL OXIDE 4003

FIG. 42

4043 2nd POLY GATE

TiSi₂ IN WORDLINES

4035

n+ POLY IN WORD LINES 4037

4031 { 4037 4035 4033

4043 4007 4023 4017

4027

4025 {

4003

INTER-LEVEL OXIDE

4019 4009 4017

A B



FIG. 43

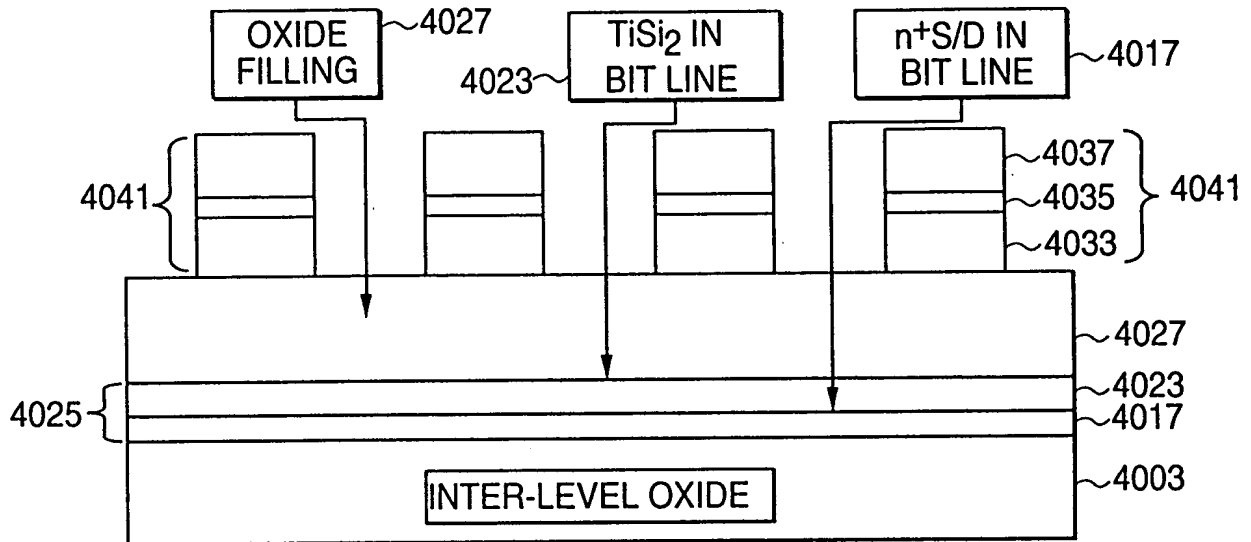


FIG. 44

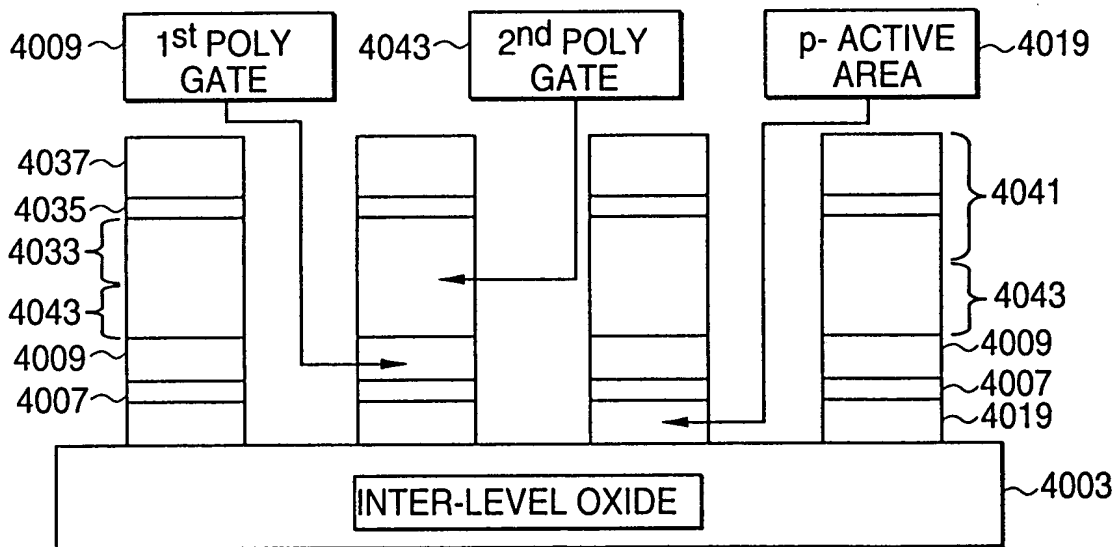




FIG. 45

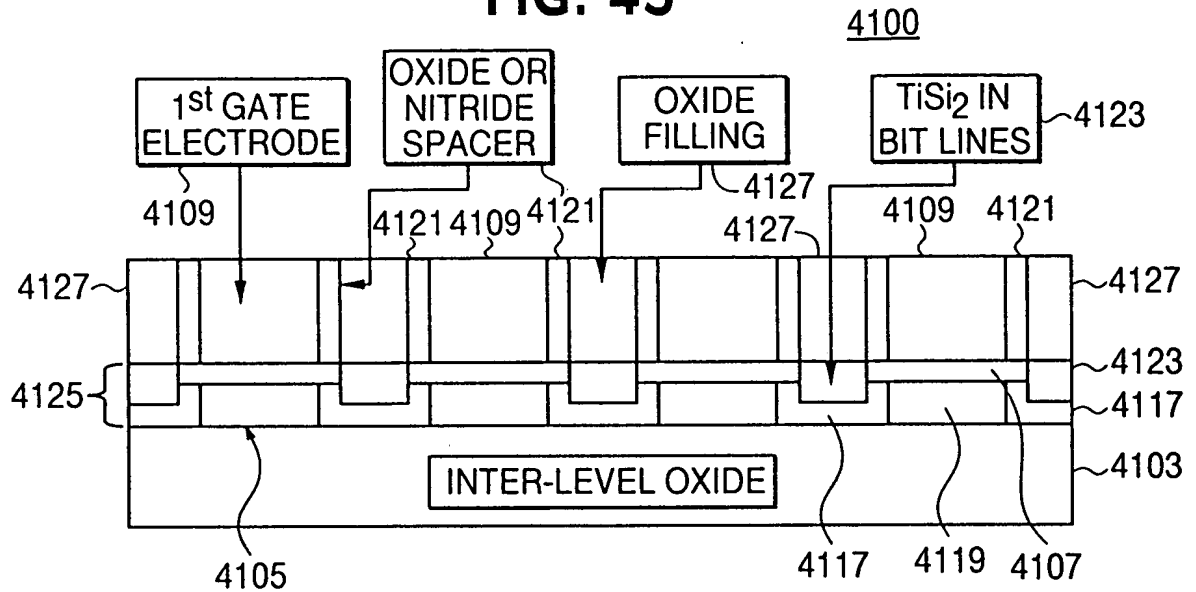


FIG. 46

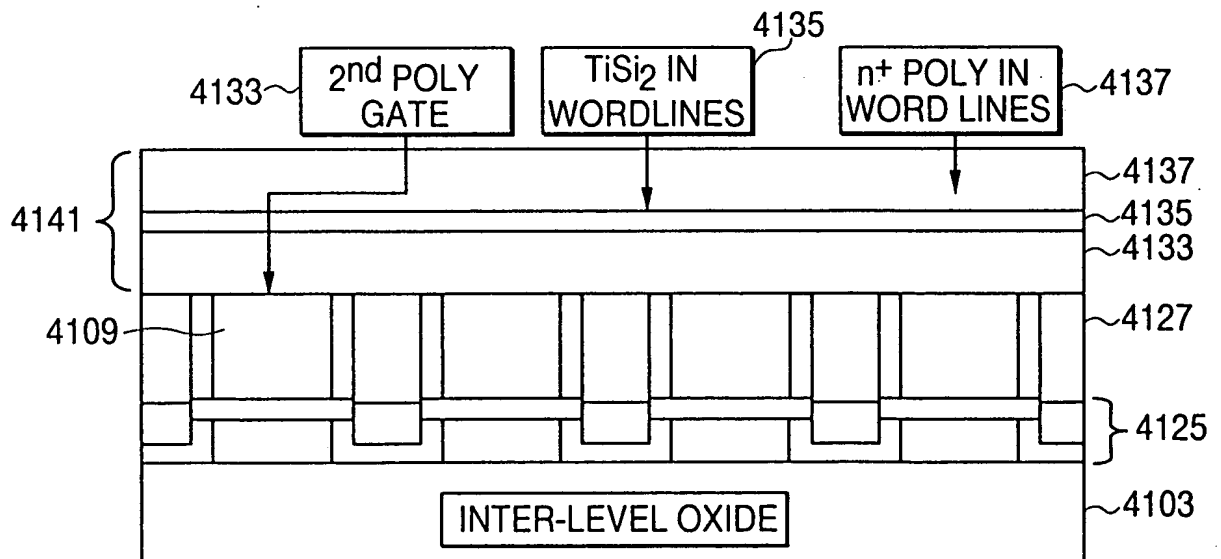




FIG. 47

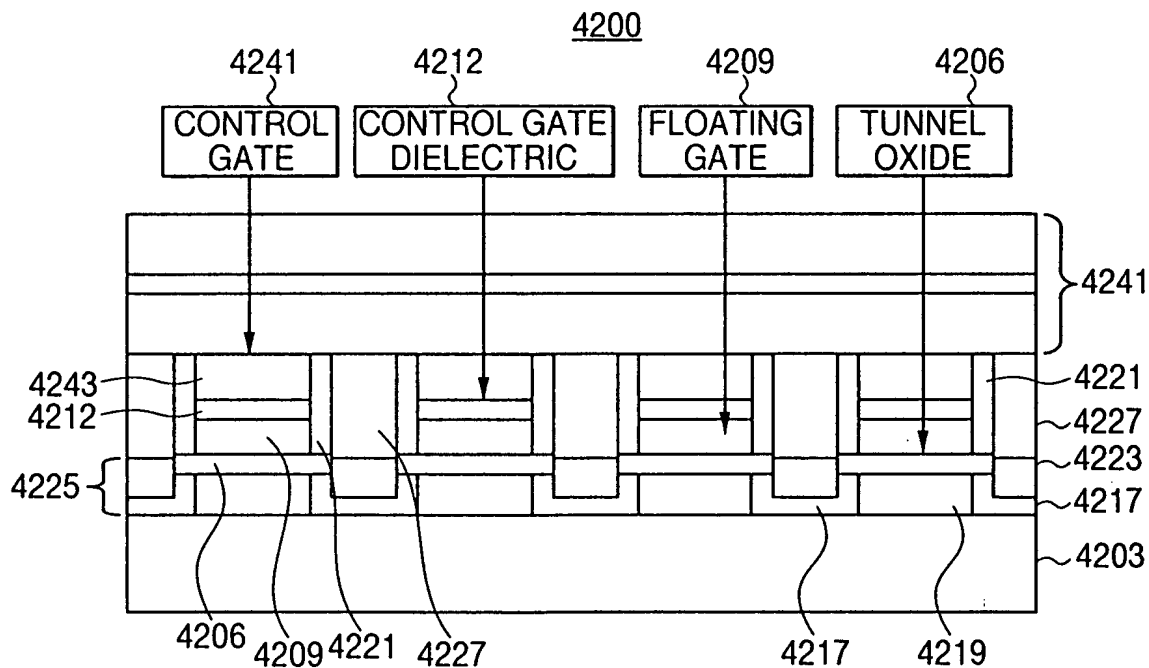


FIG. 48A

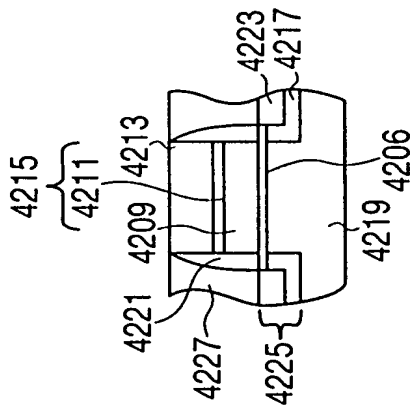


FIG. 48B

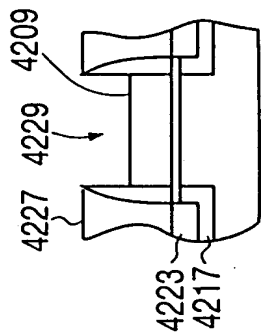


FIG. 48C

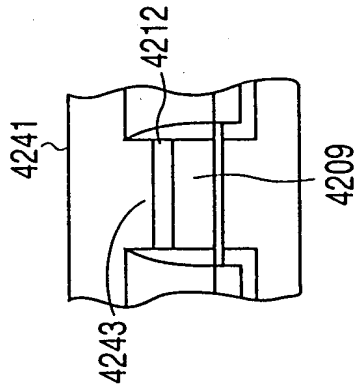


FIG. 49A

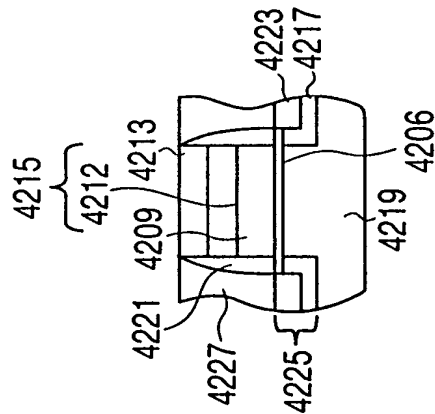


FIG. 49B

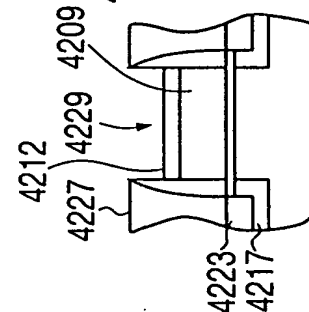


FIG. 49C

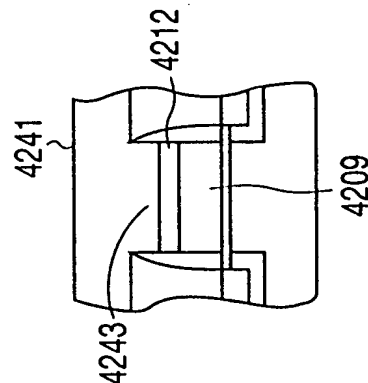




FIG. 50

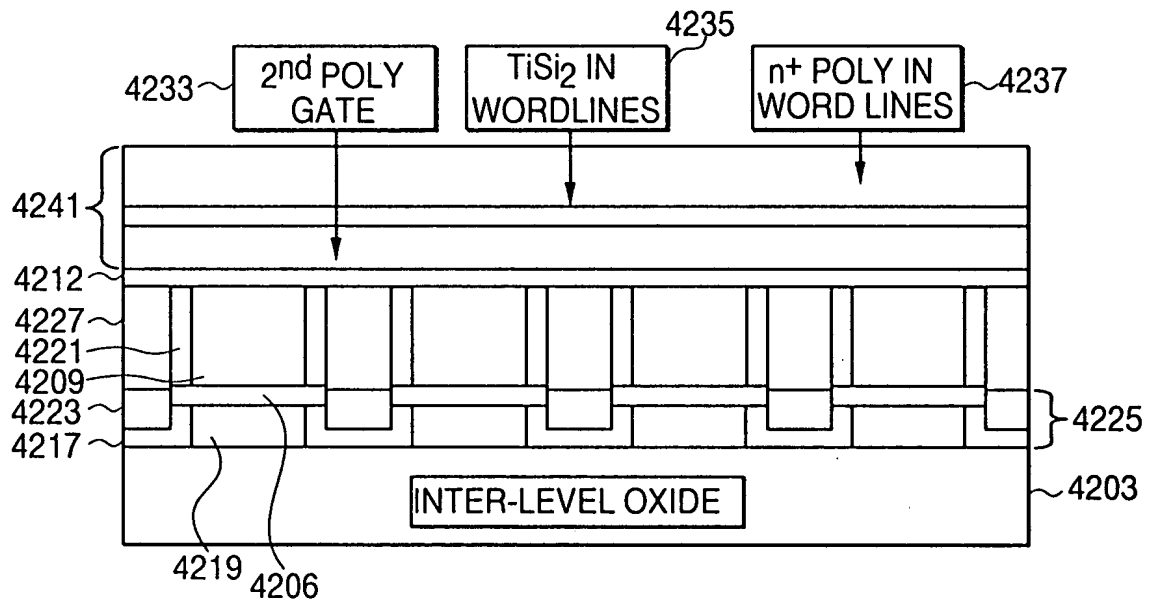




FIG. 51

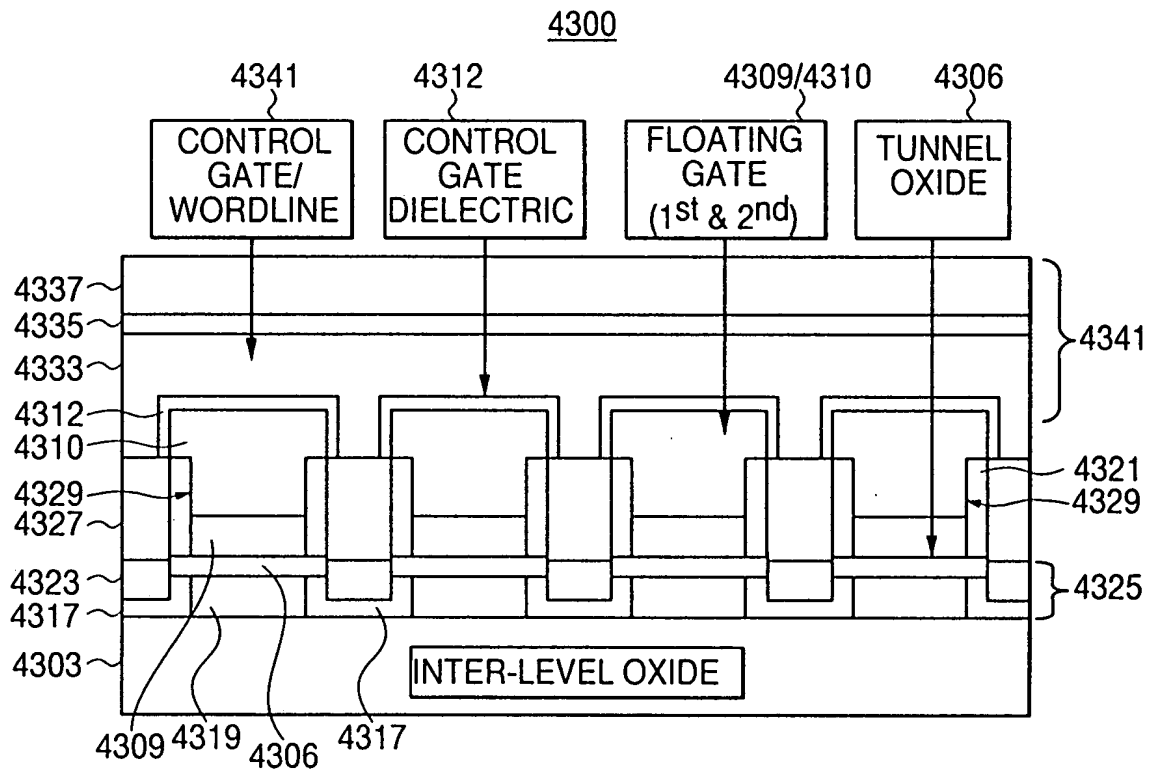




FIG. 52

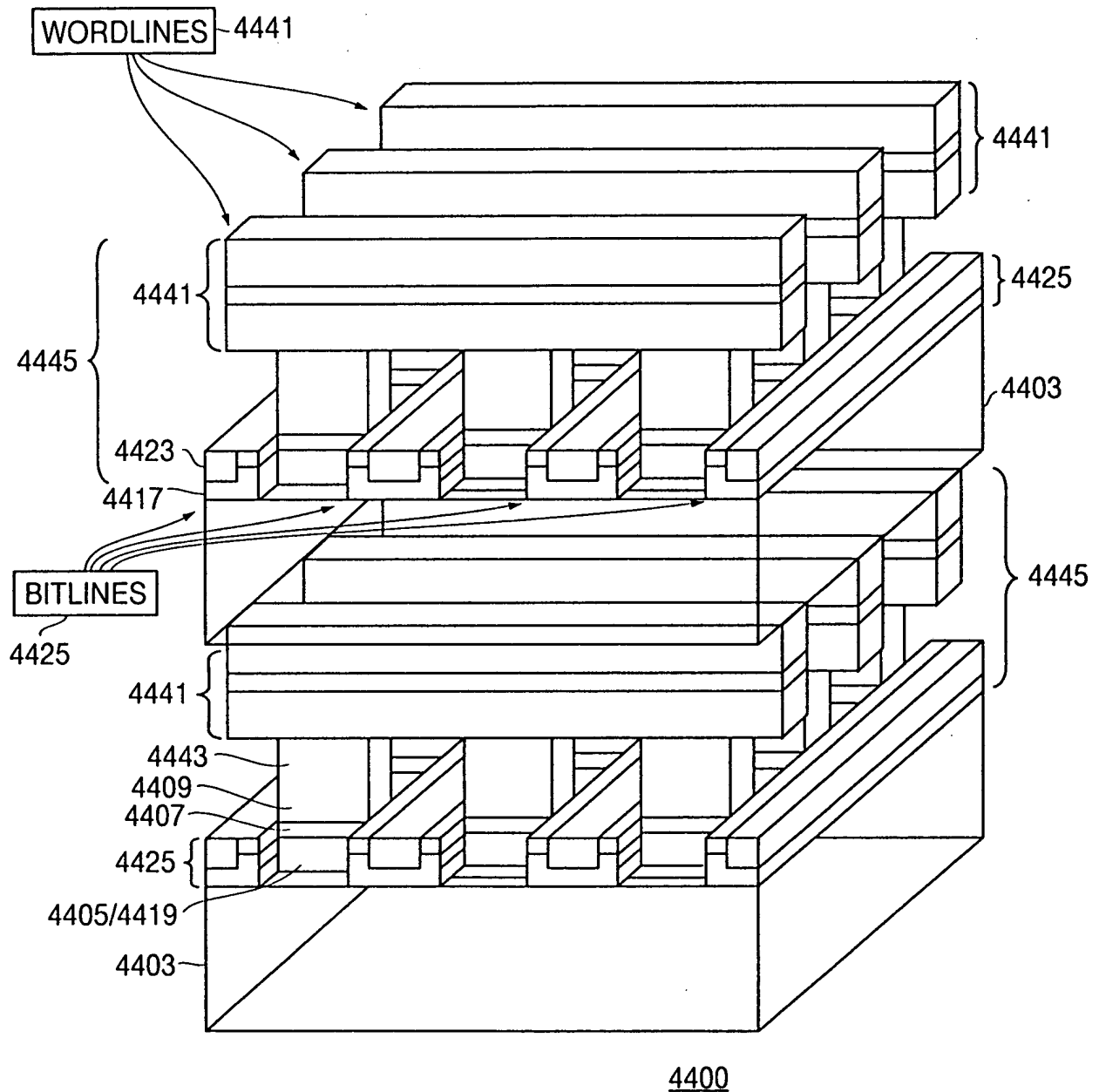




FIG. 53

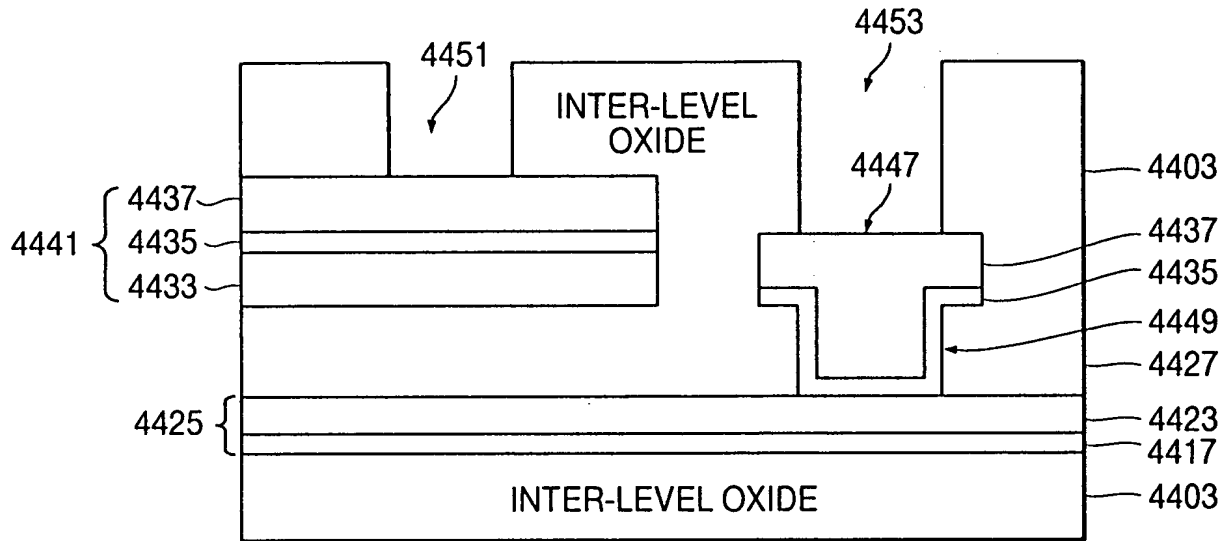


FIG. 54

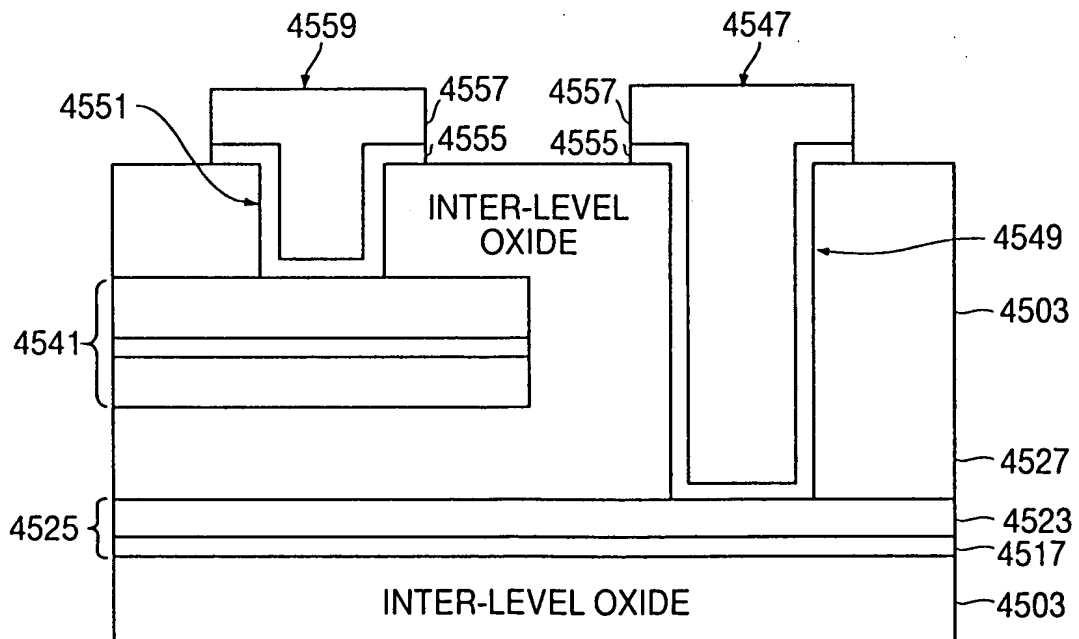


FIG. 55

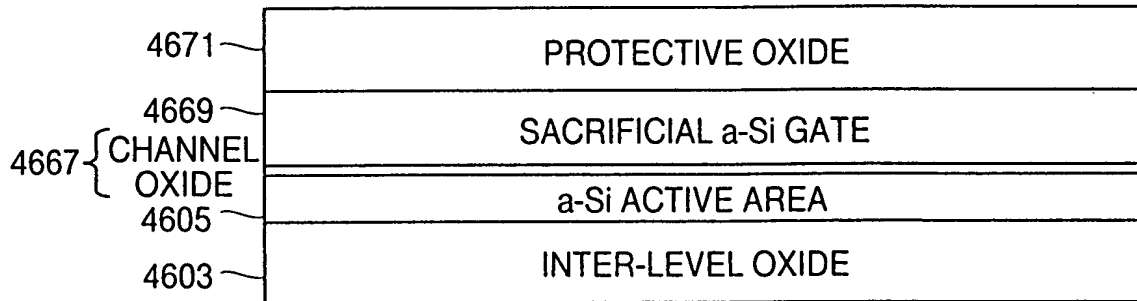


FIG. 56

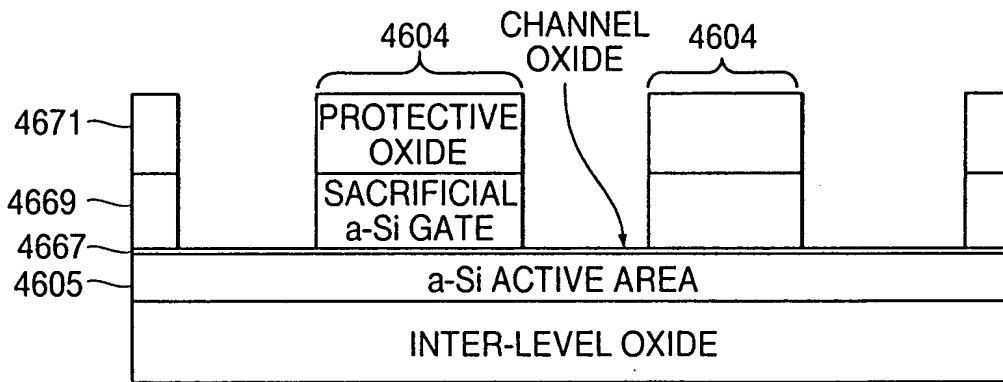


FIG. 57

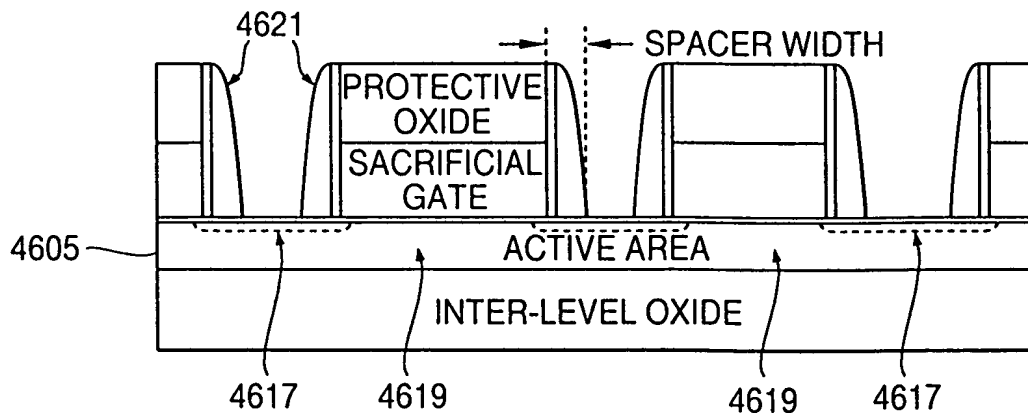


FIG. 58

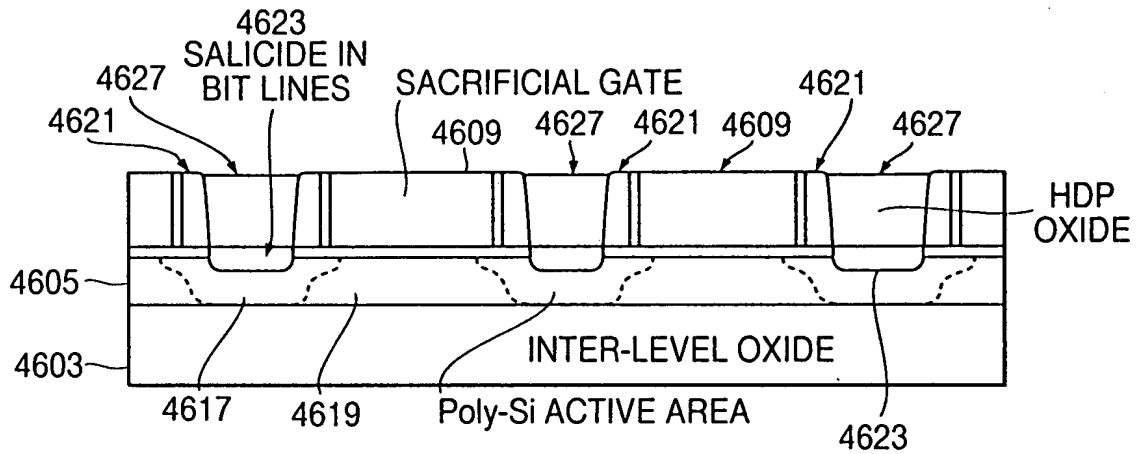


FIG. 59

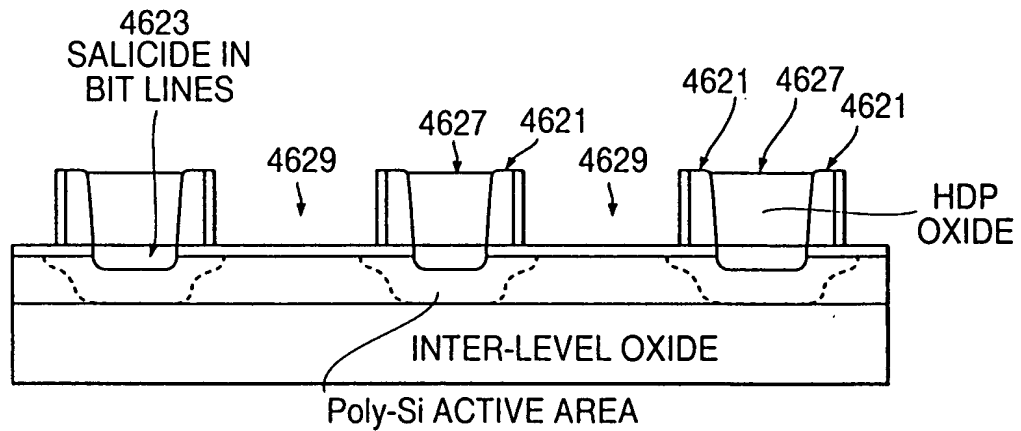


FIG. 60

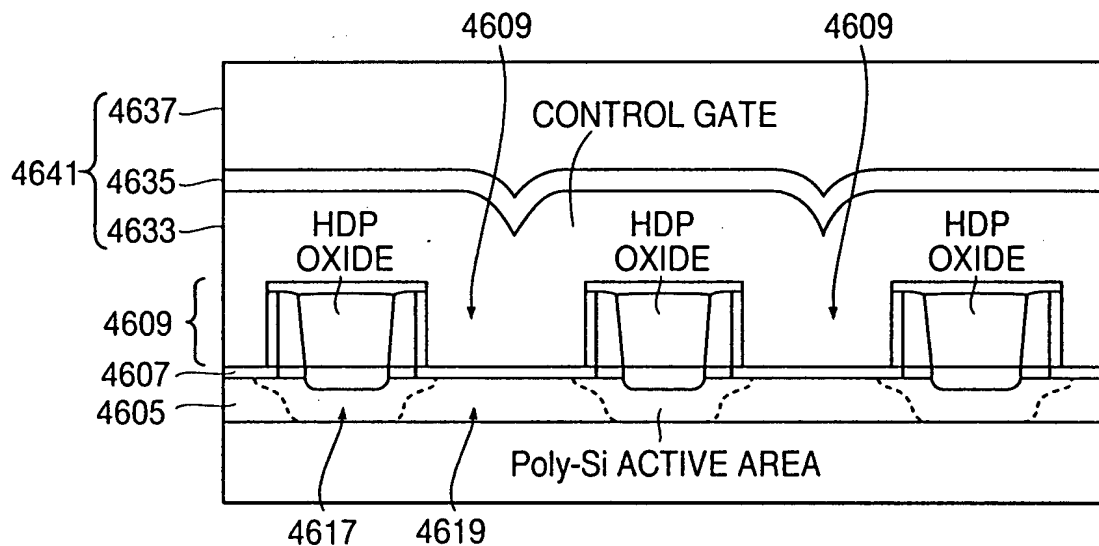


FIG. 61

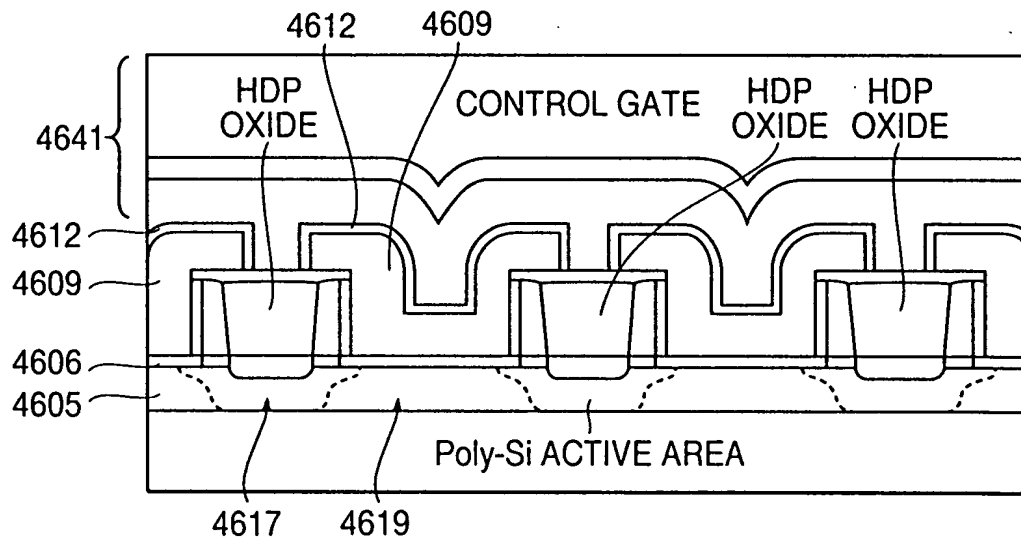




FIG. 62

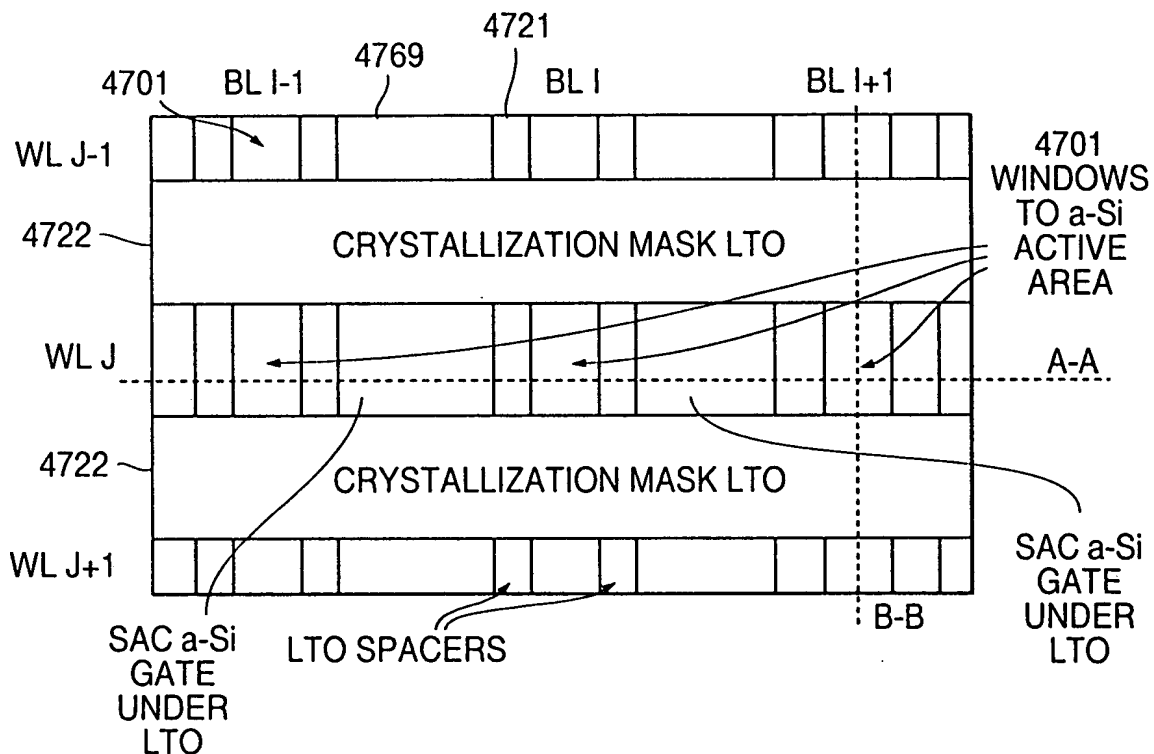




FIG. 63

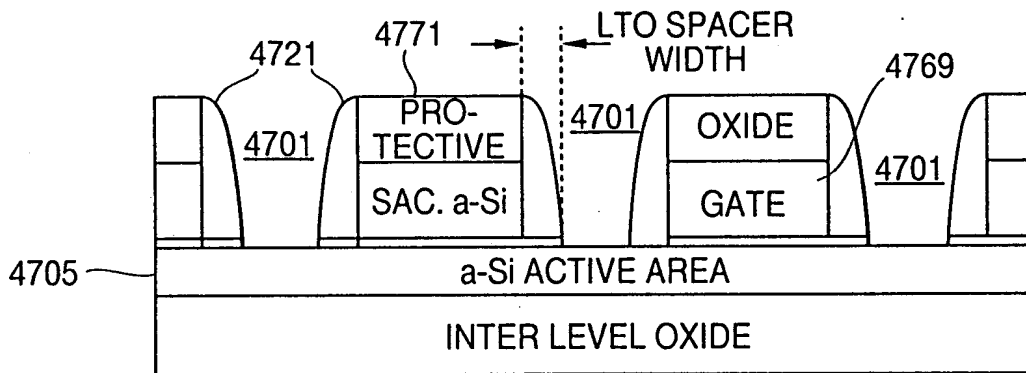


FIG. 64

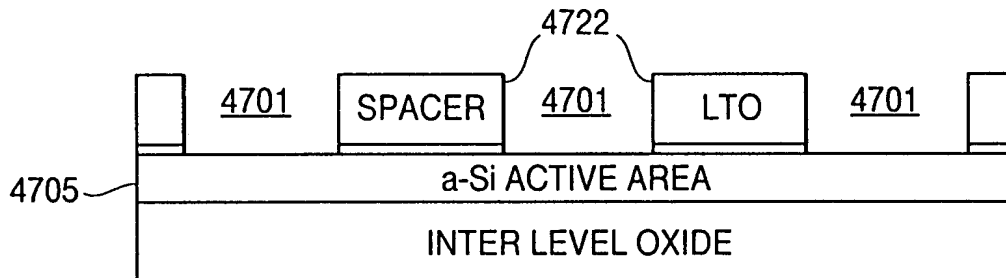
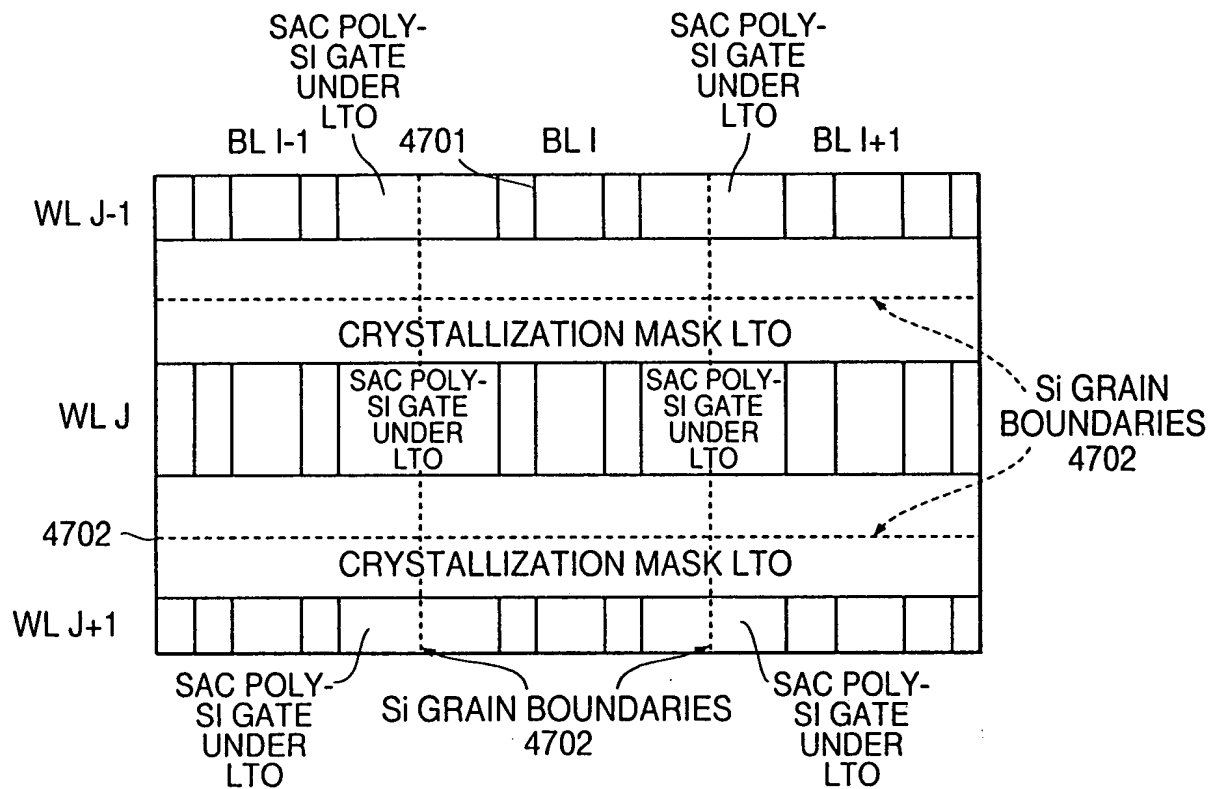




FIG. 65



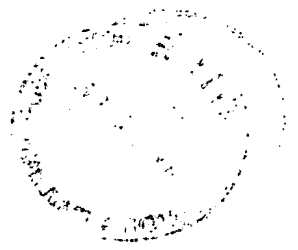


FIG. 66

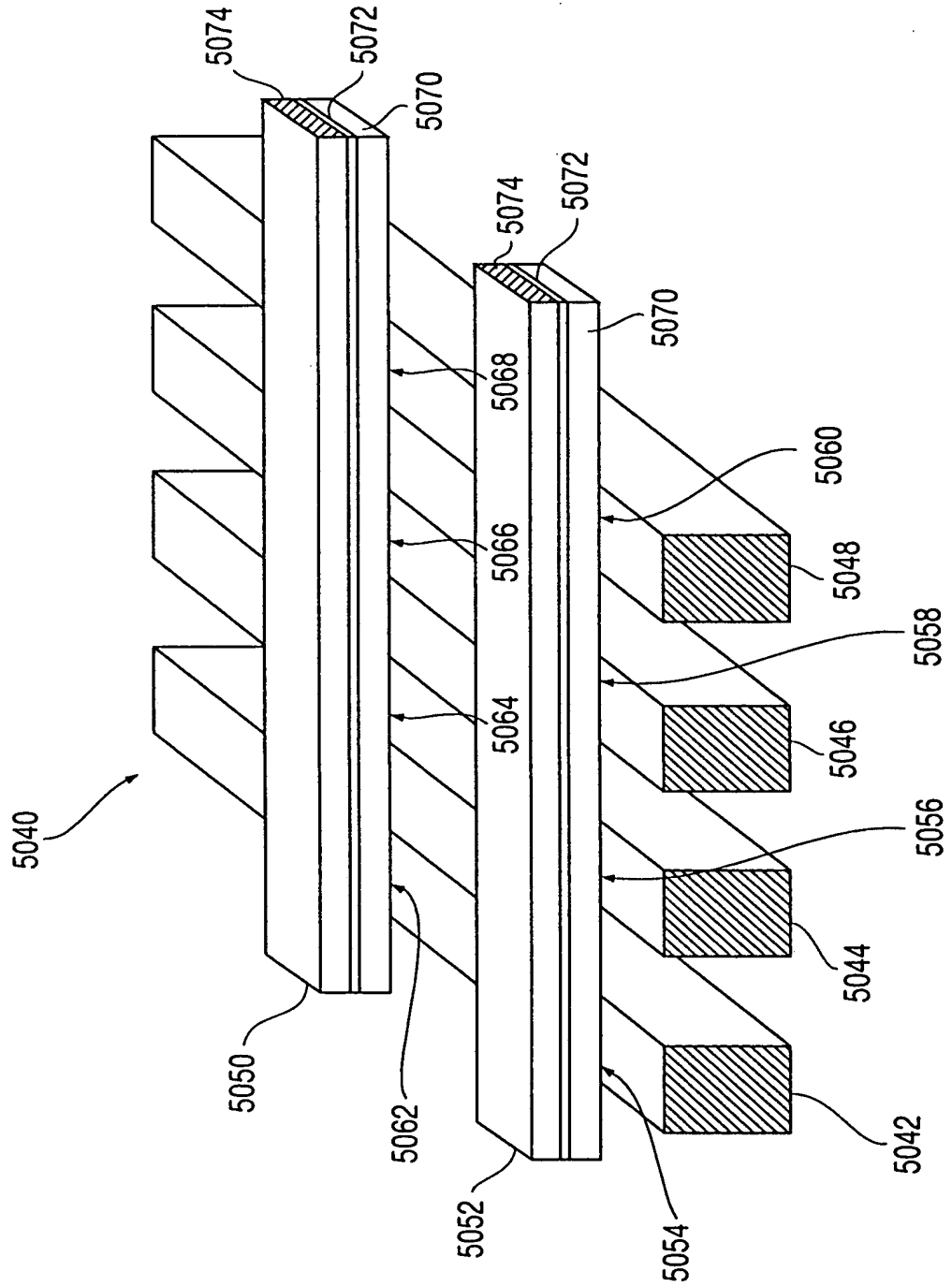


FIG. 66

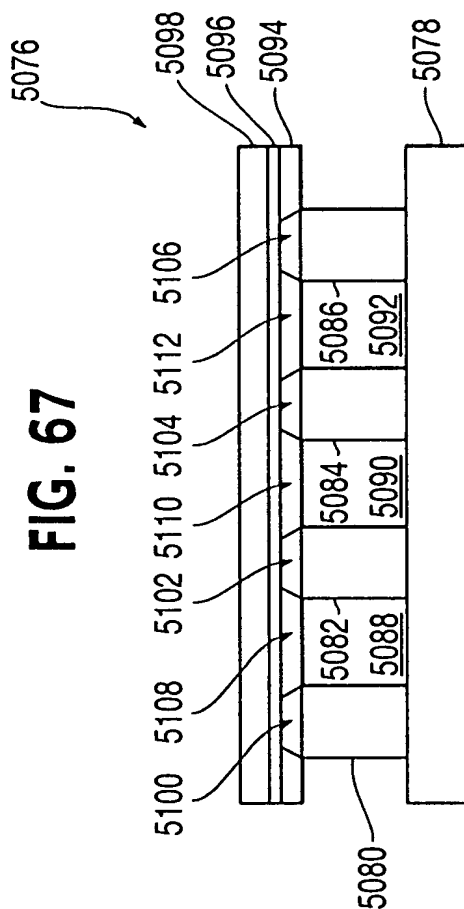
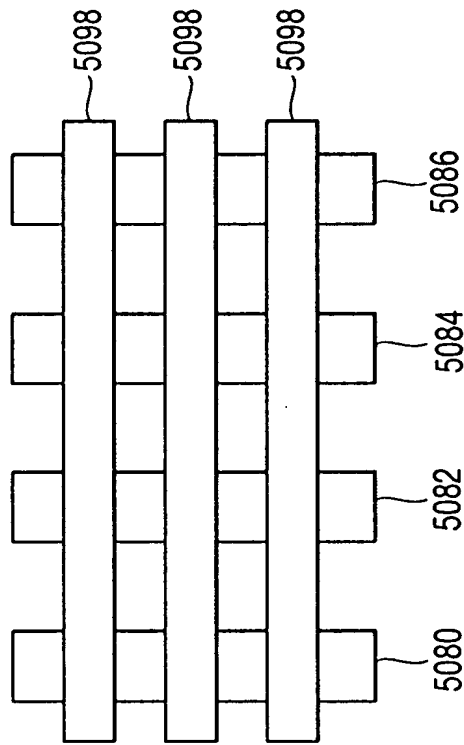


FIG. 67



FIG. 68



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FIG. 69

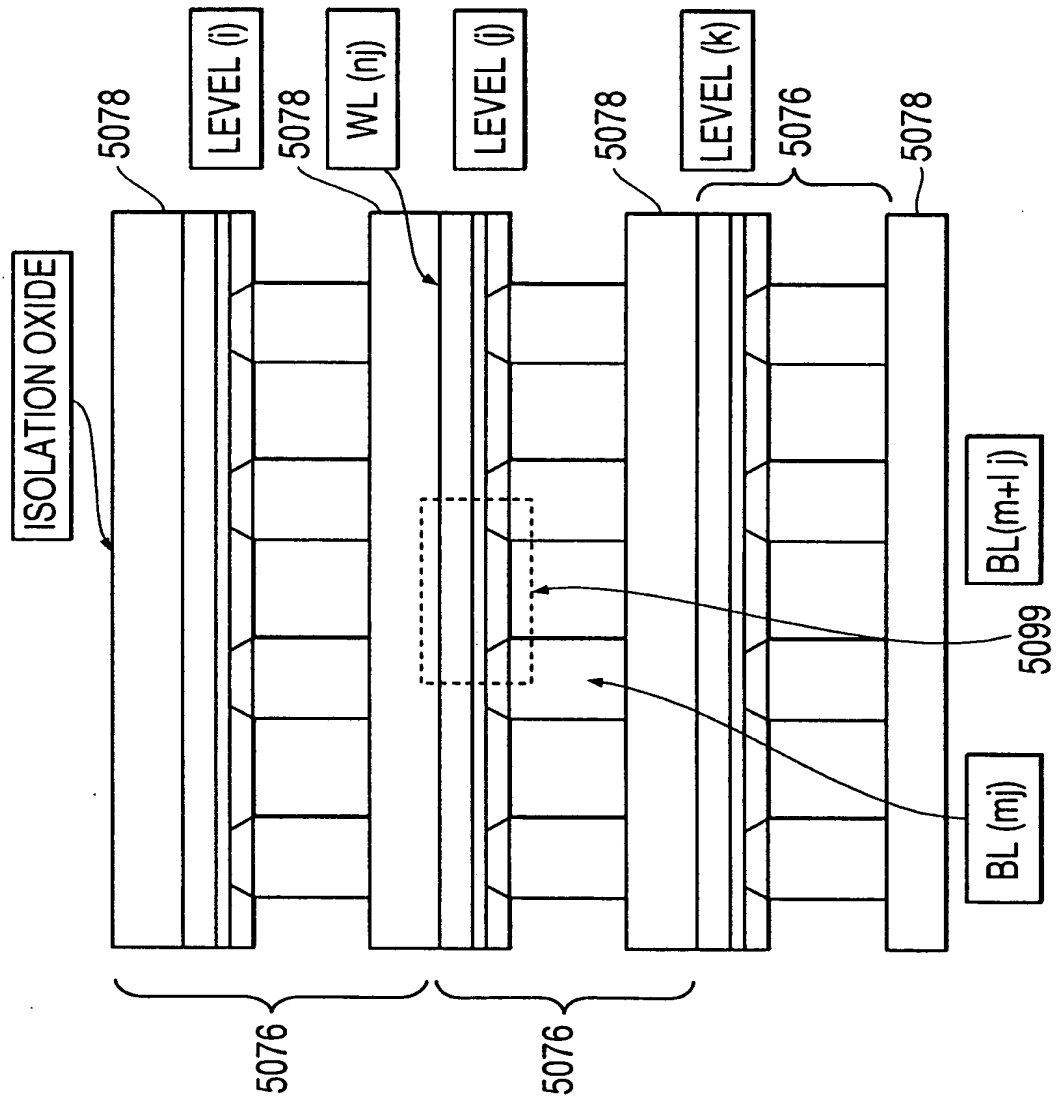




FIG. 70

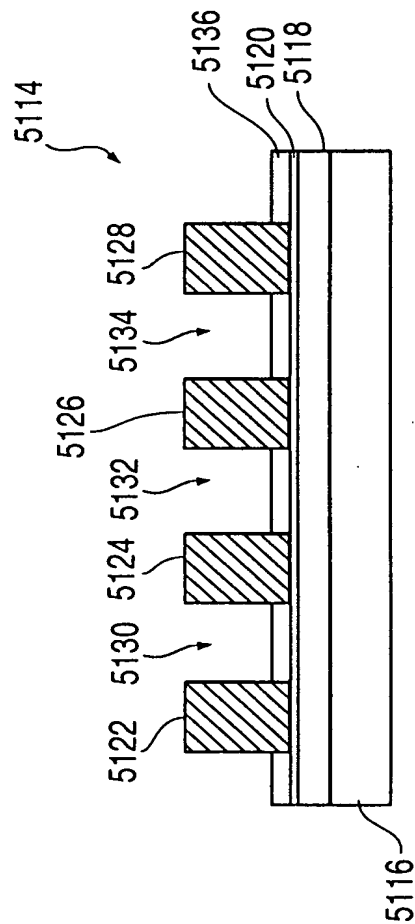


FIG. 70



FIG. 71

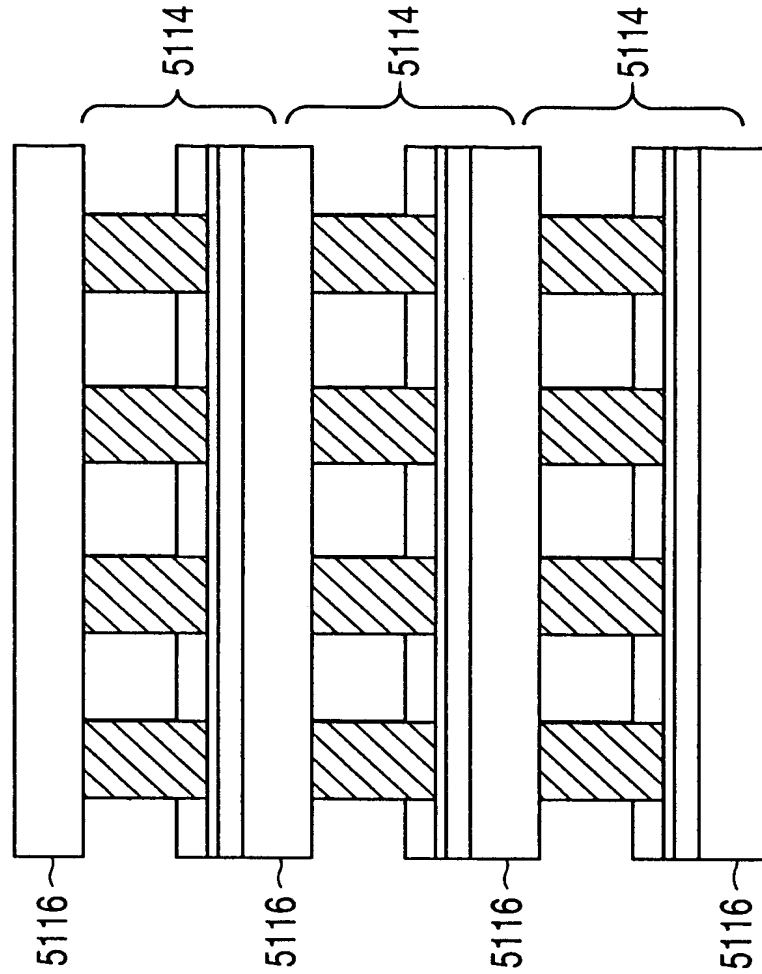




FIG. 72

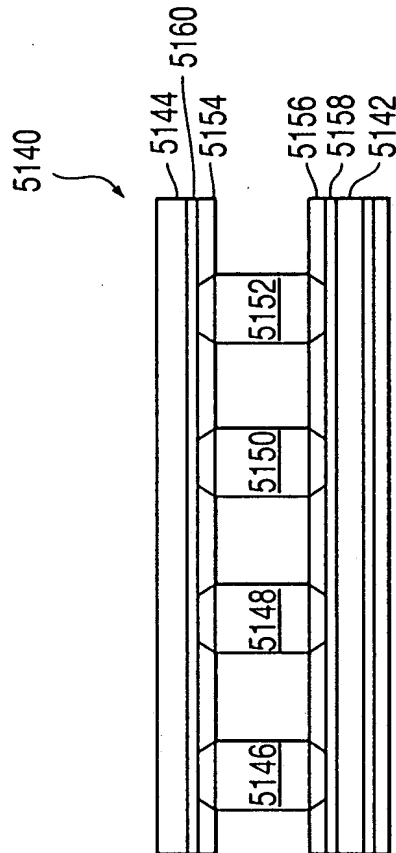




FIG. 73

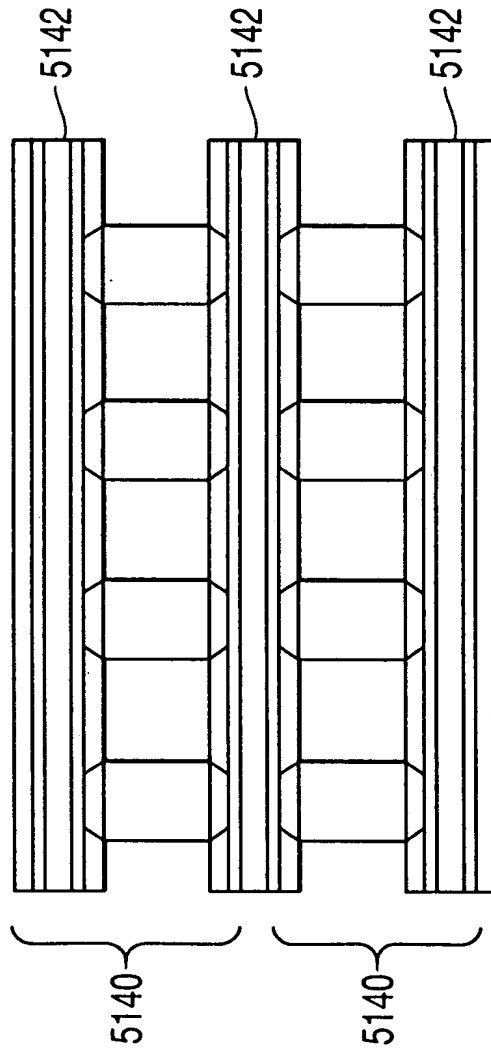


FIG. 73



FIG. 74

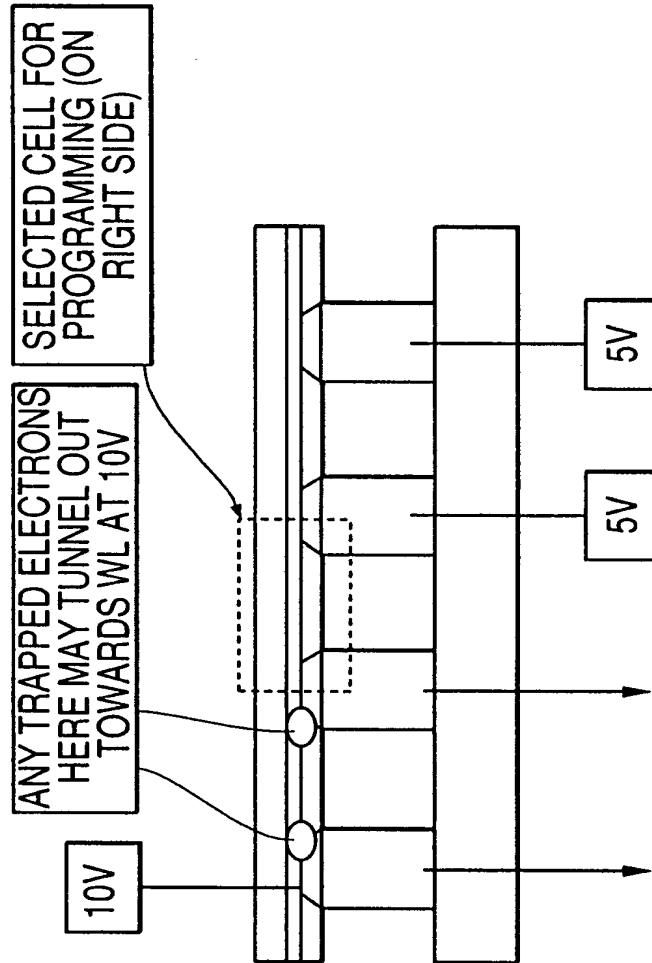


FIG. 74



FIG. 75

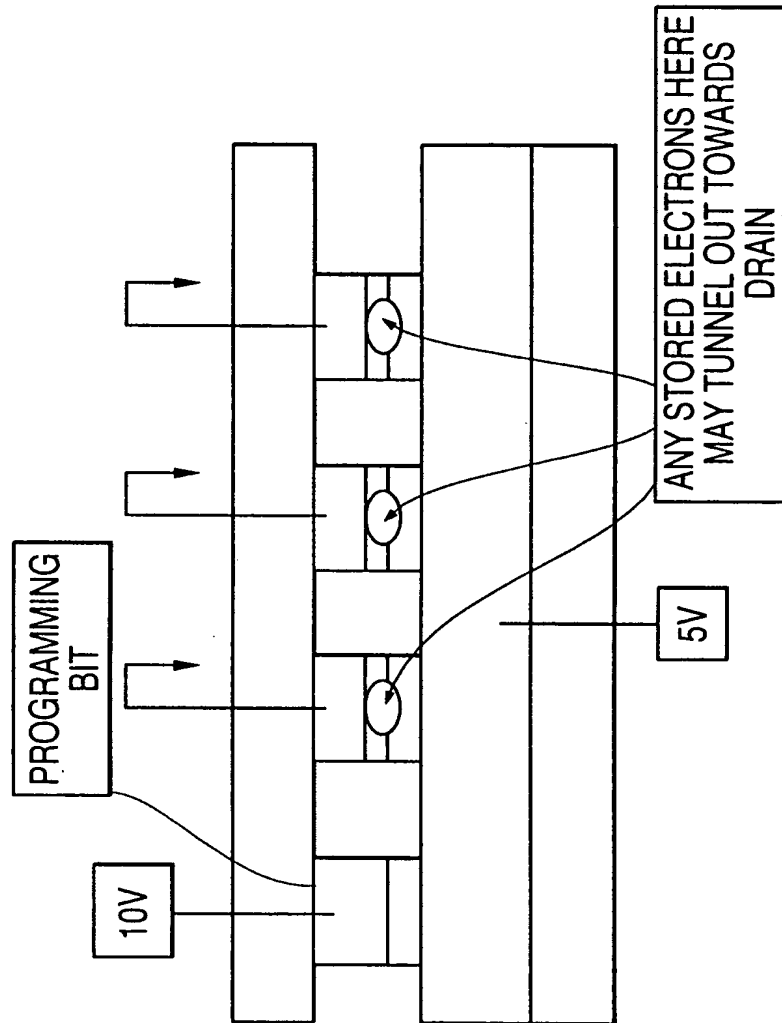
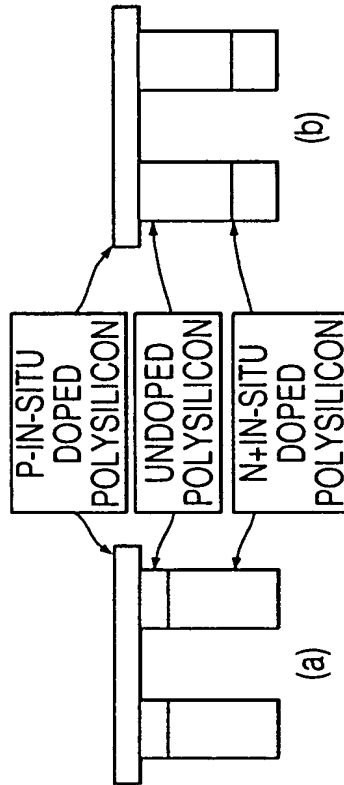




FIG. 76



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FIG. 77

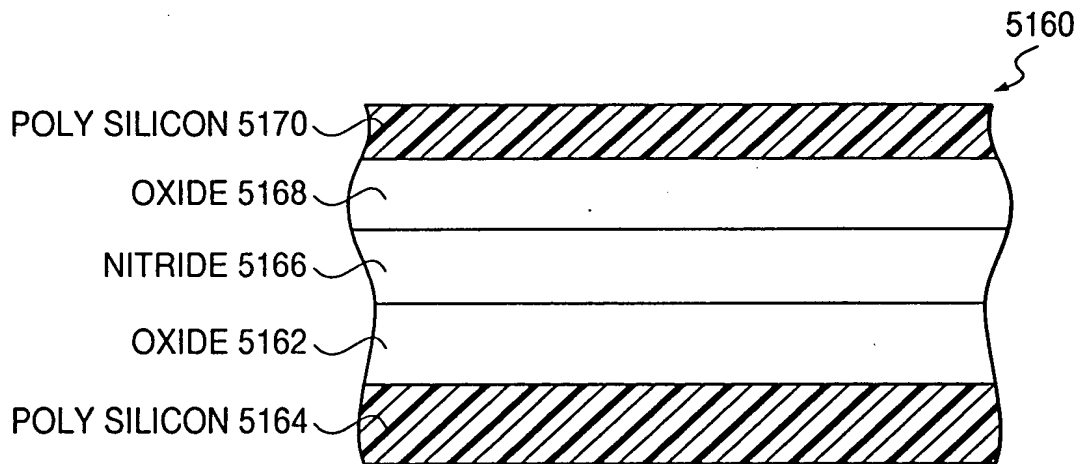


FIG. 80

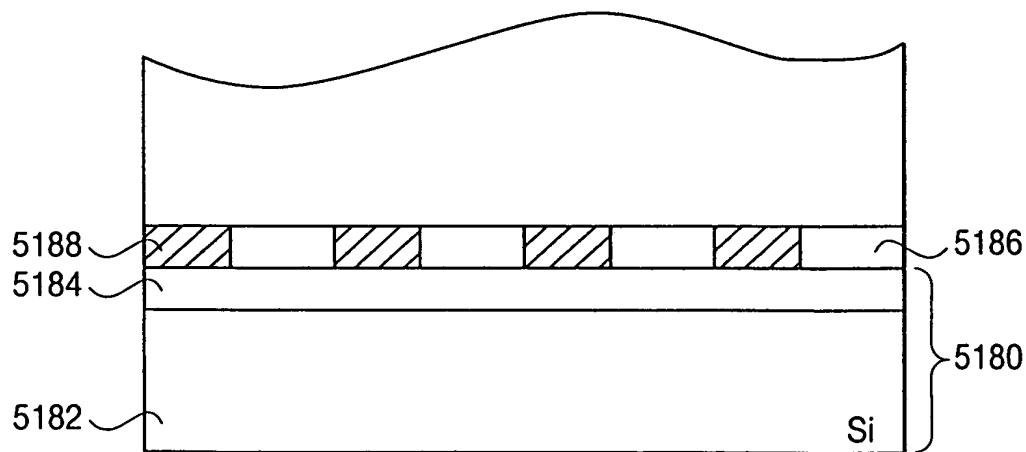




FIG. 78

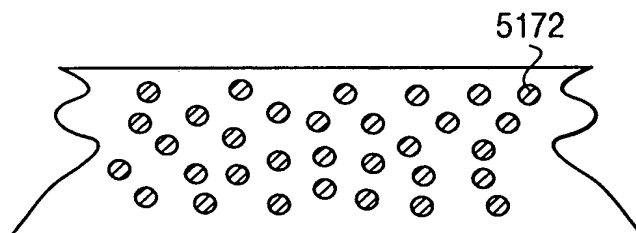
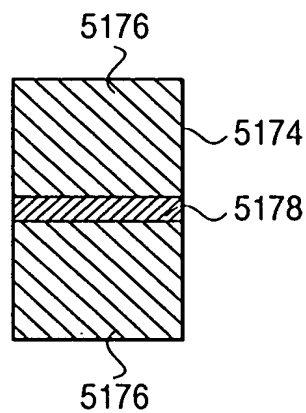


FIG. 79



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FIG. 81A

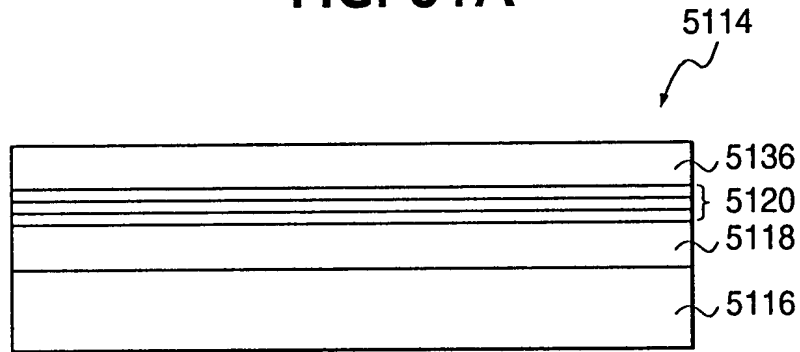


FIG. 81B

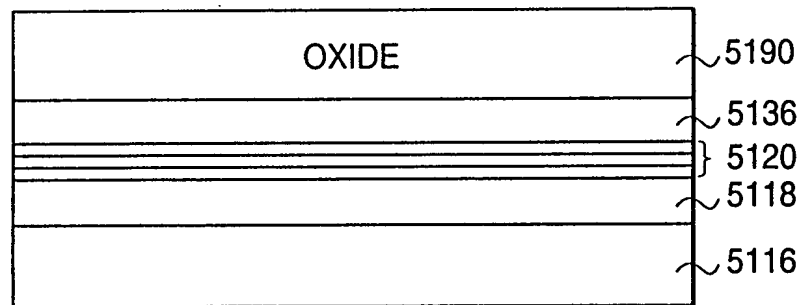
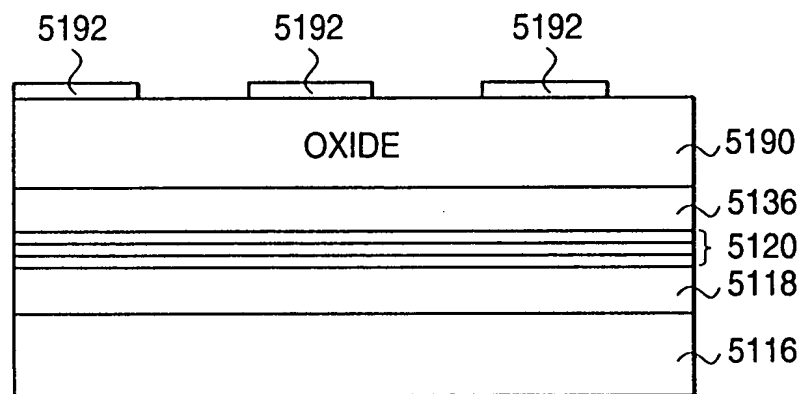


FIG. 81C



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FIG. 81D

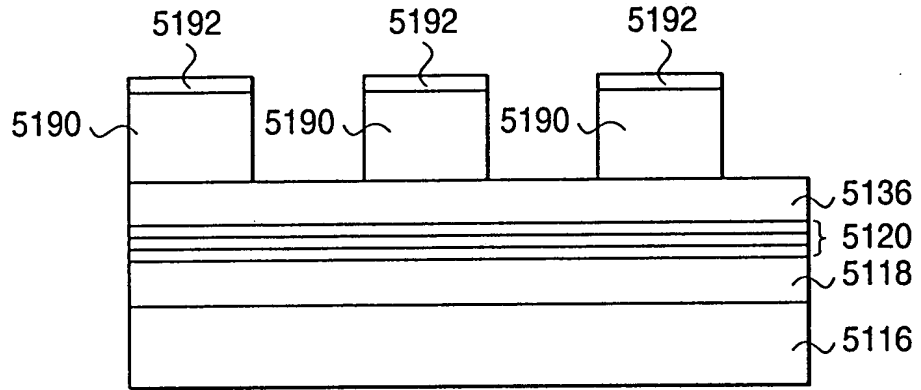


FIG. 81E

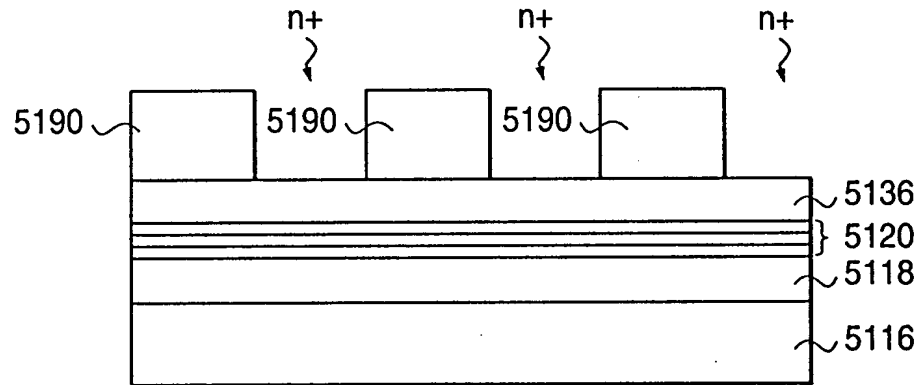
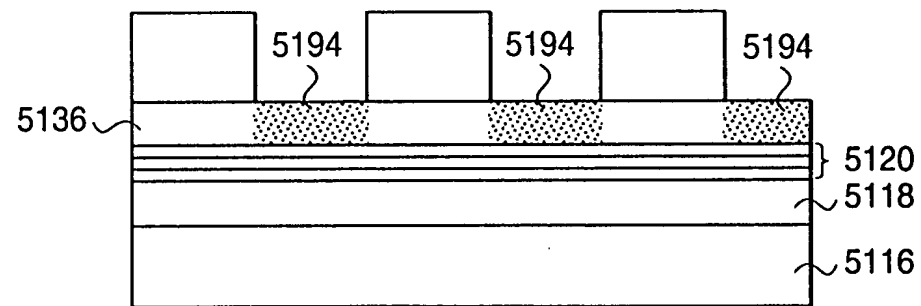


FIG. 81F



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FIG. 81G

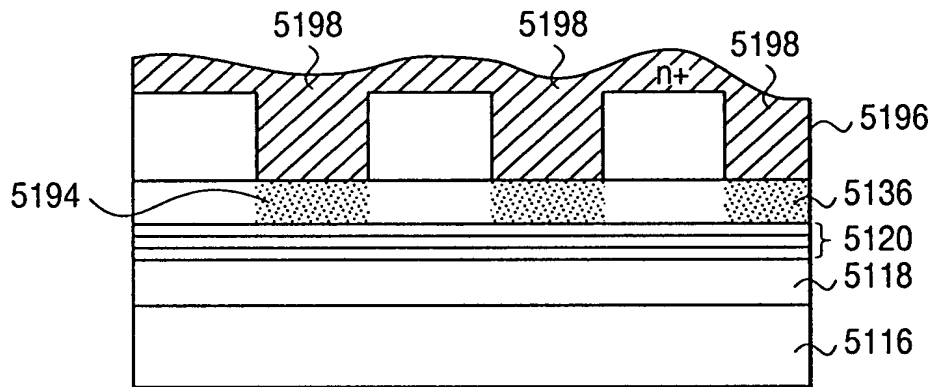


FIG. 81H

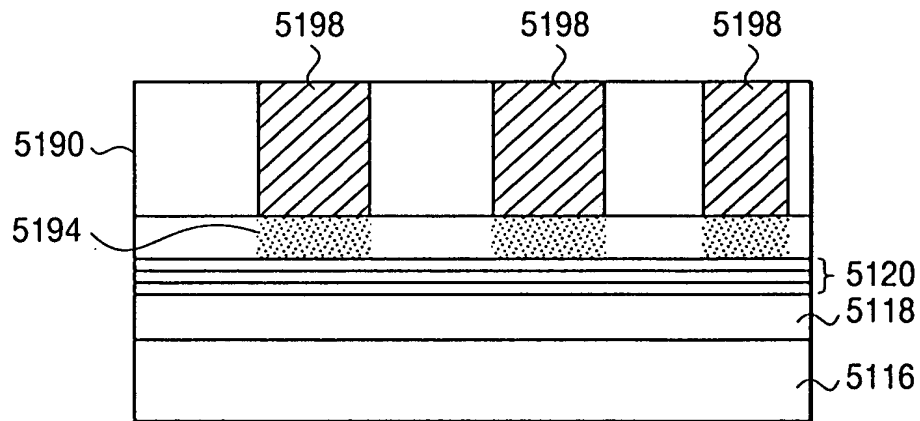




FIG. 82A

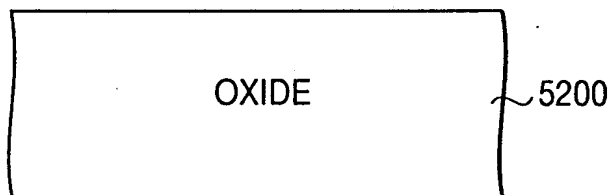


FIG. 82B

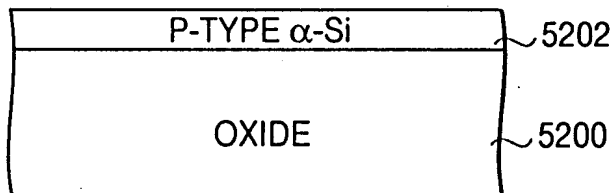


FIG. 82C

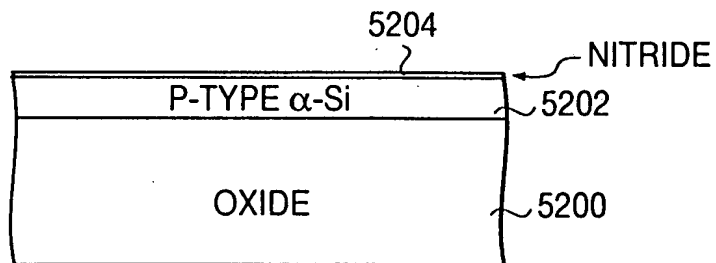




FIG. 82D

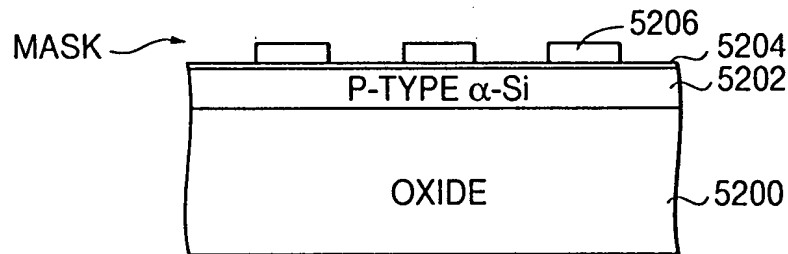


FIG. 82E

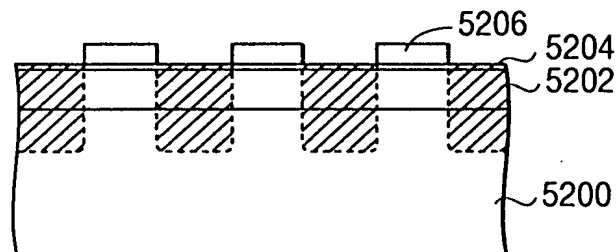


FIG. 82F

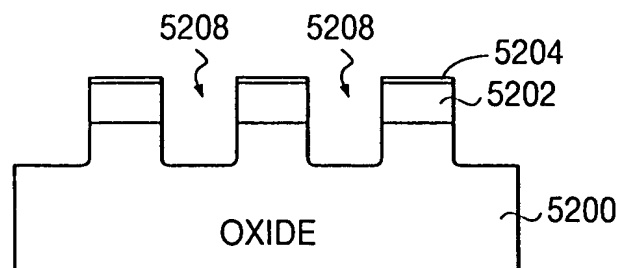


FIG. 82G

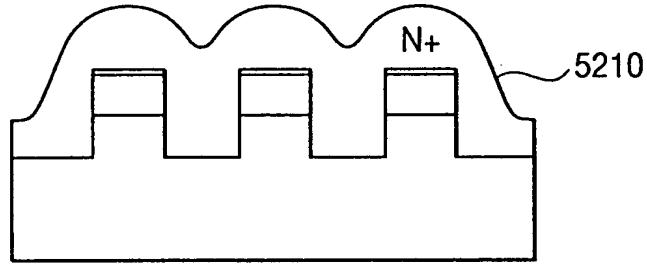


FIG. 82H

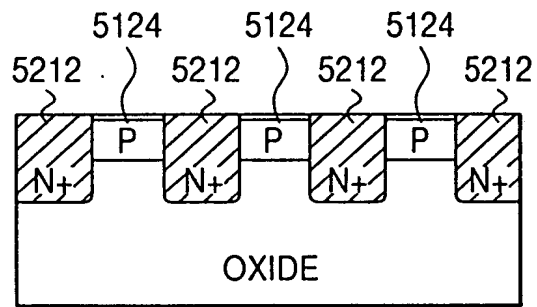
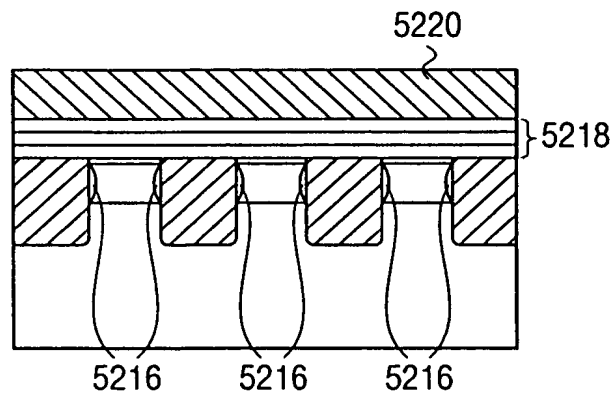


FIG. 82I



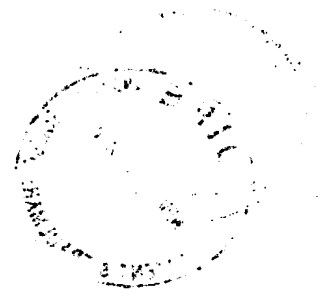


FIG. 83A

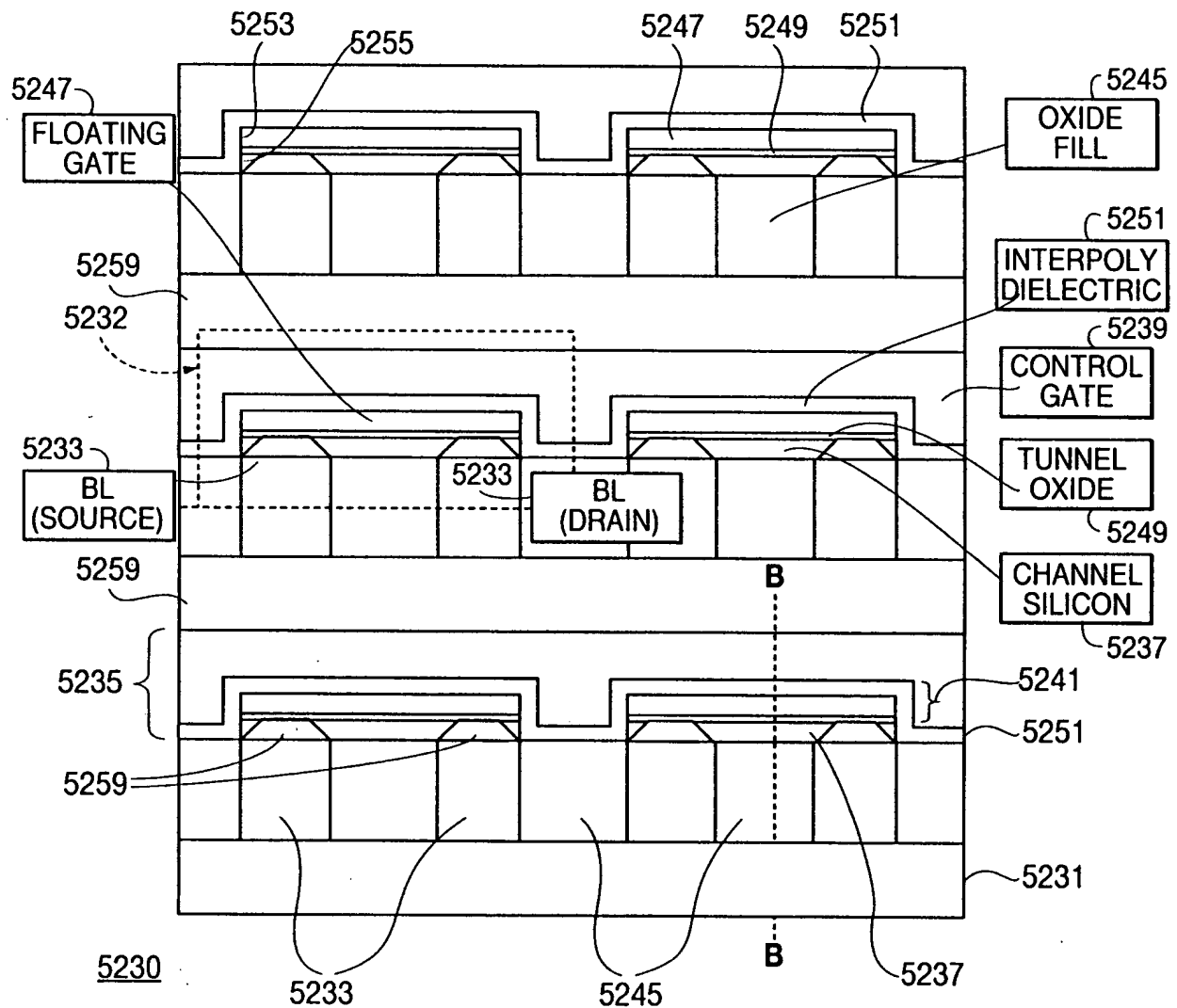




FIG. 83B

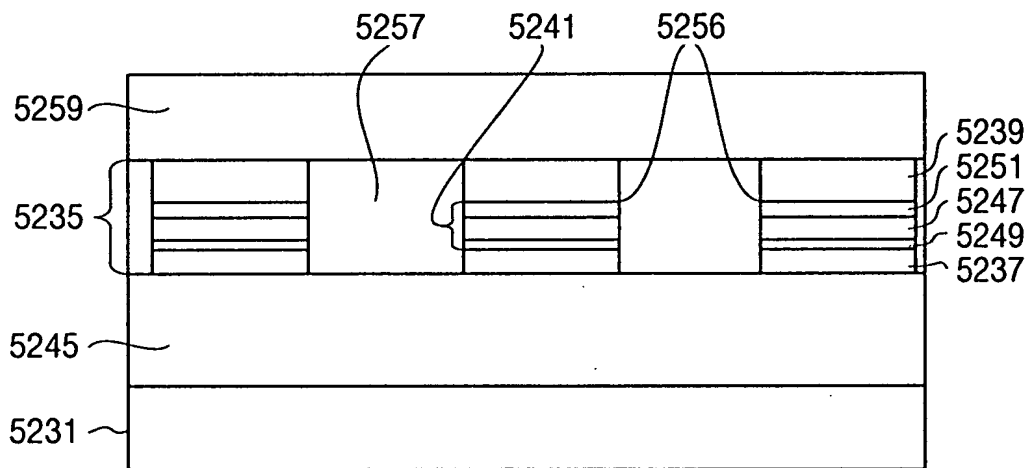




FIG. 84

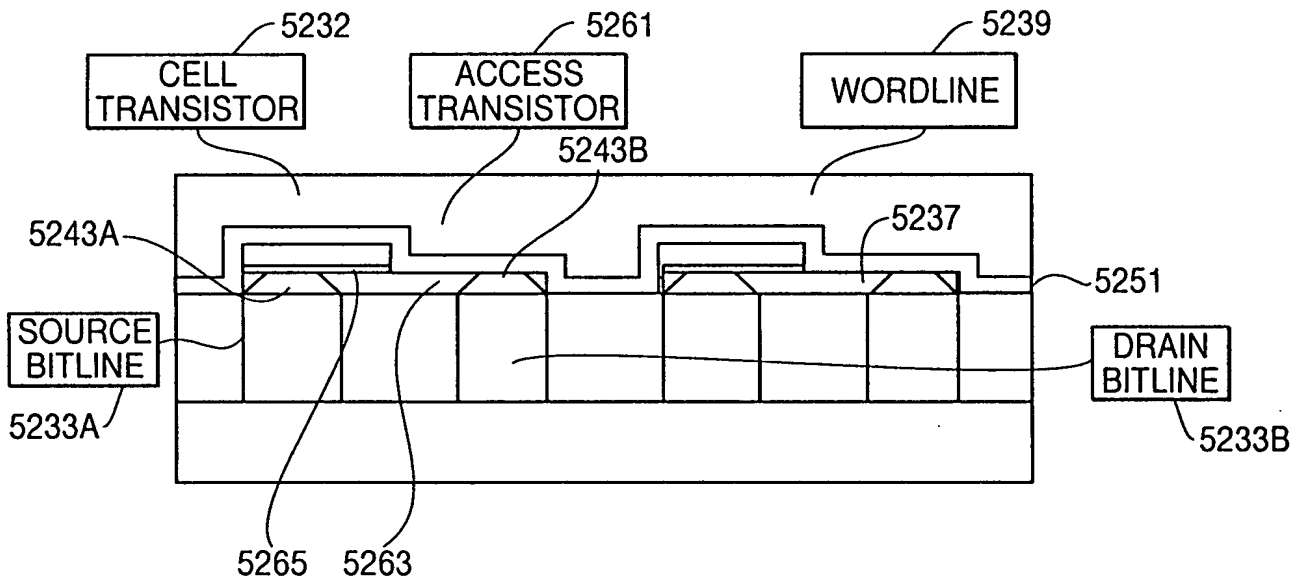




FIG. 85

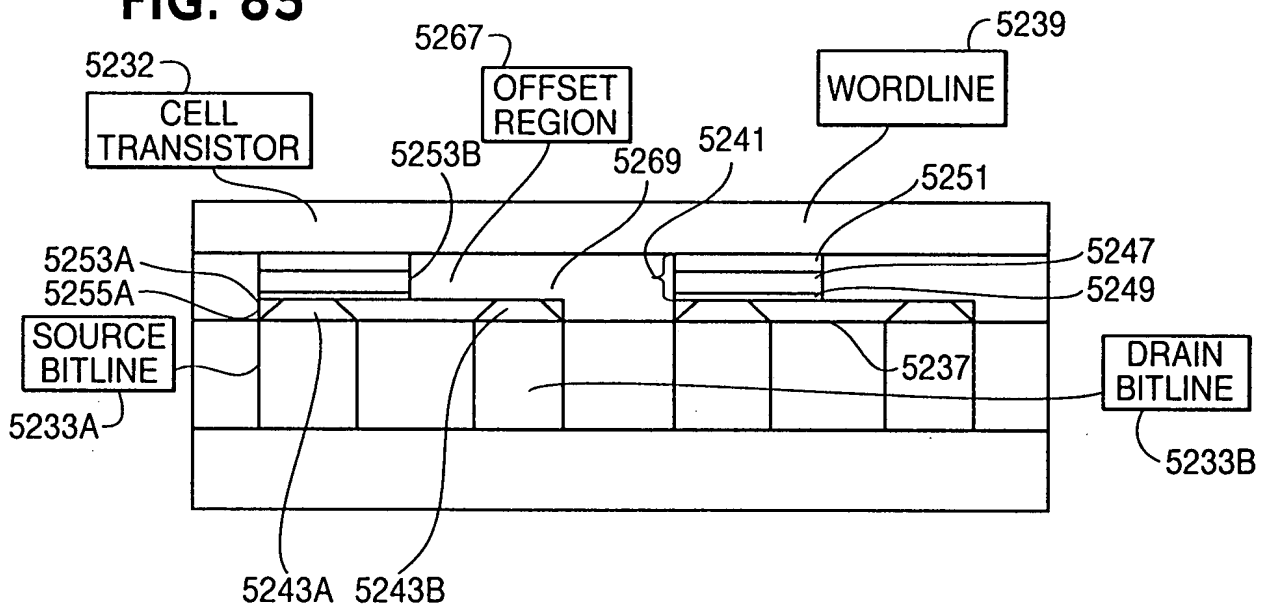




FIG. 86A

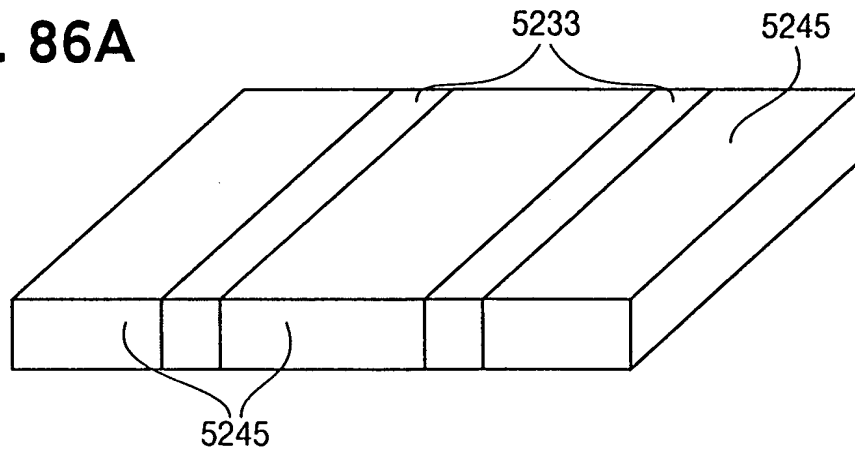


FIG. 86B

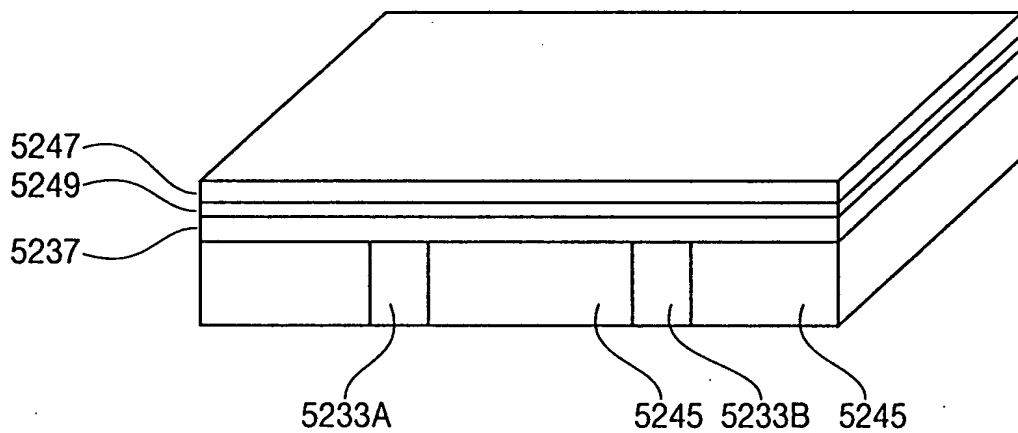
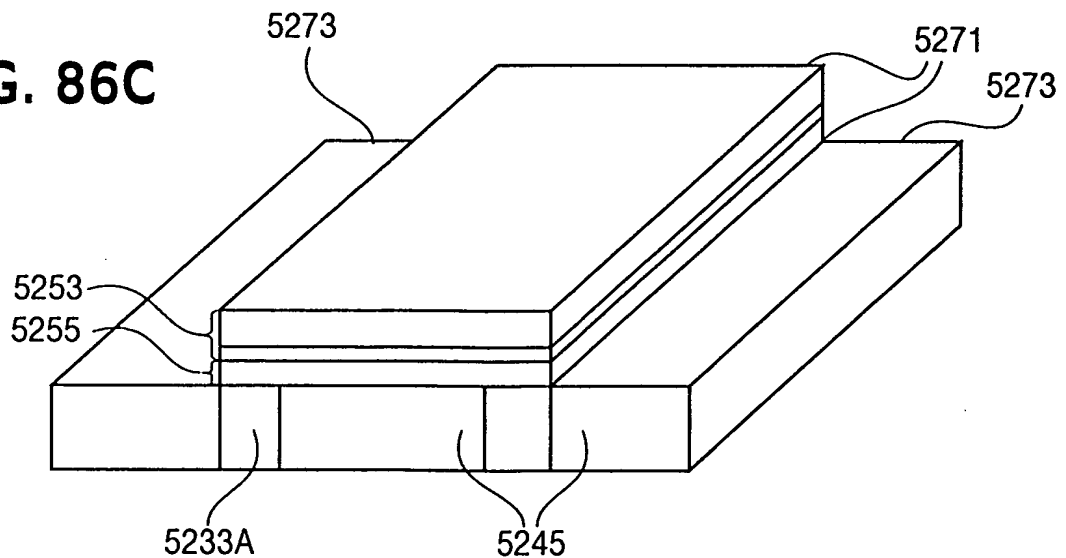
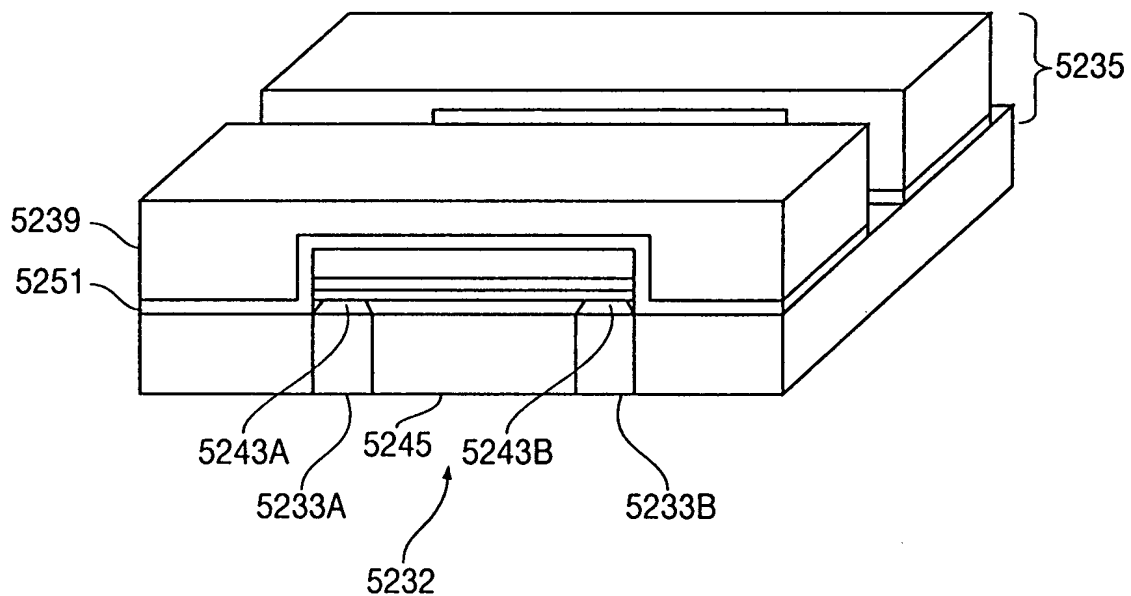


FIG. 86C



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FIG. 86D



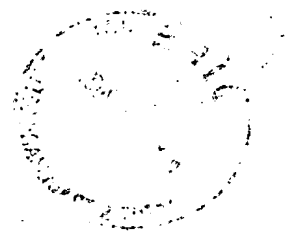


FIG. 86E

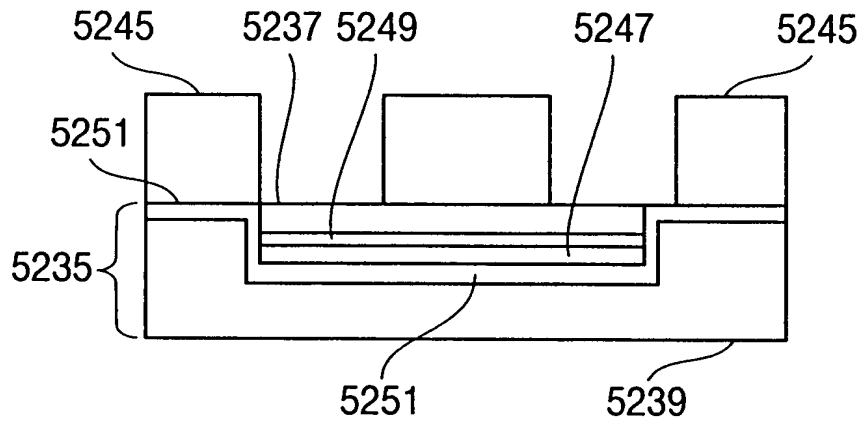


FIG. 86F

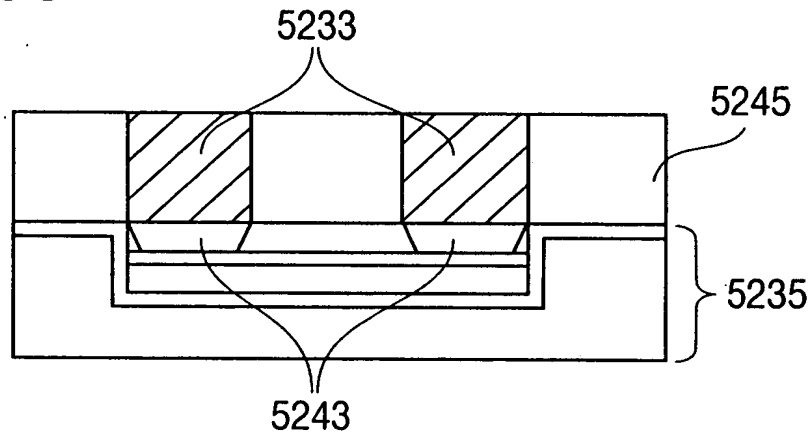




FIG. 86G

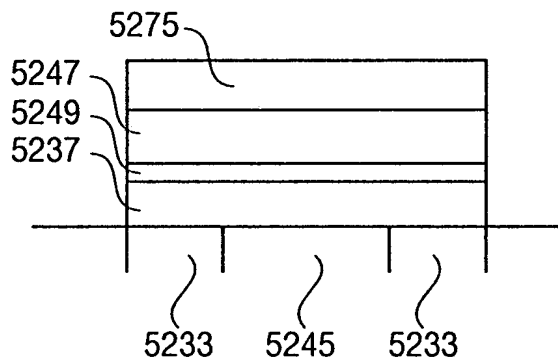


FIG. 86H

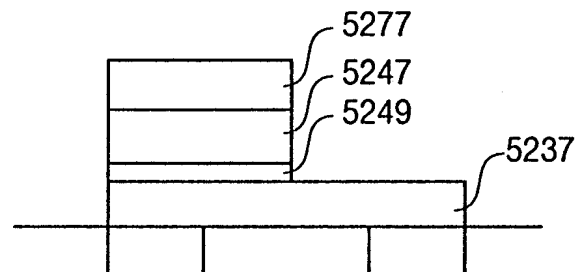


FIG. 86I

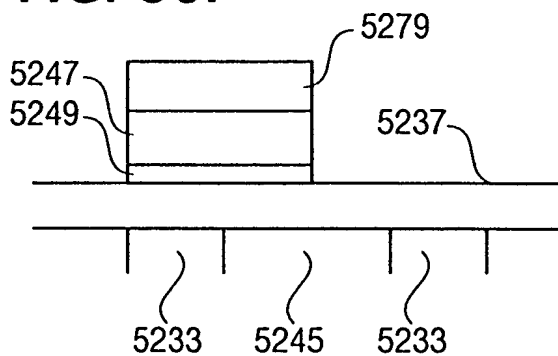


FIG. 86J

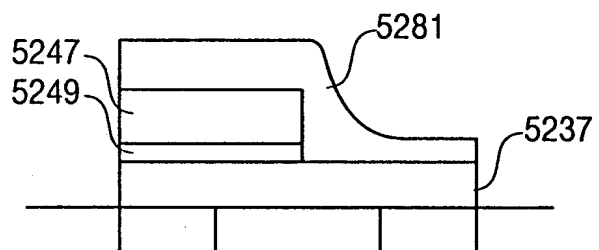




FIG. 87

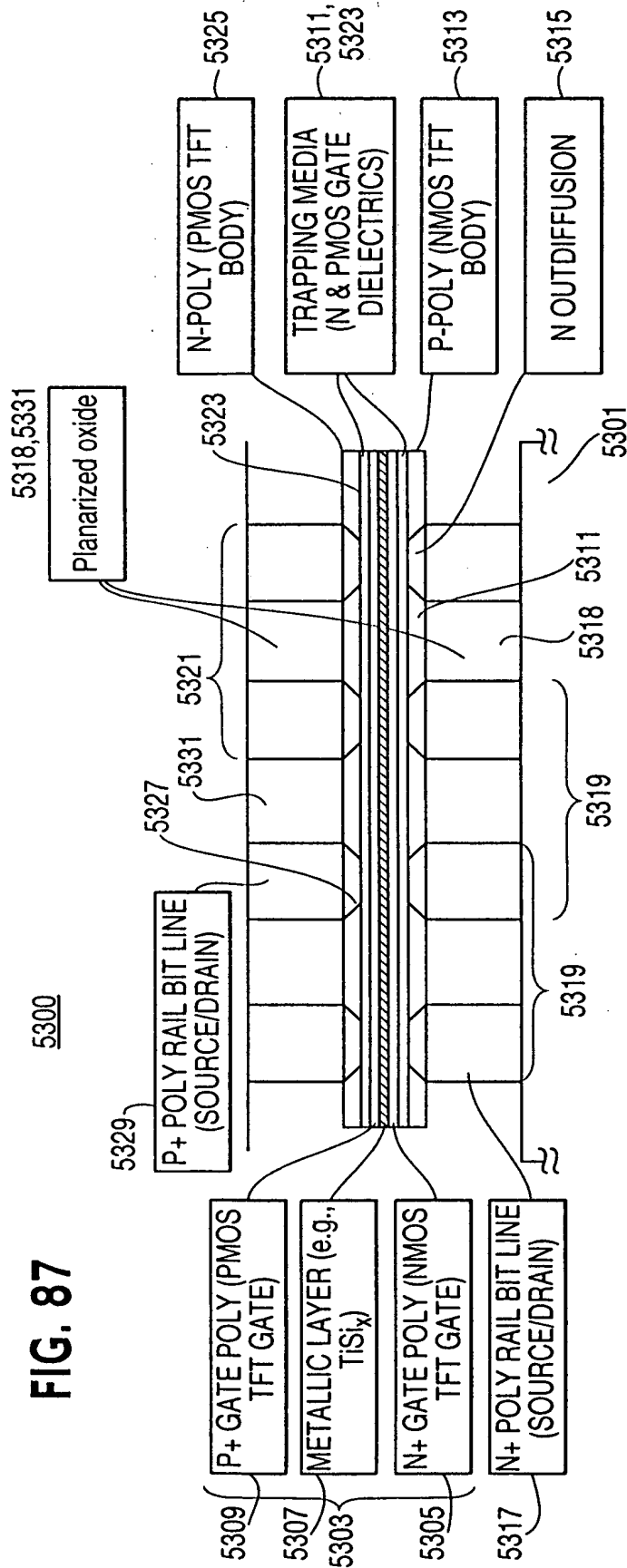




FIG. 88A

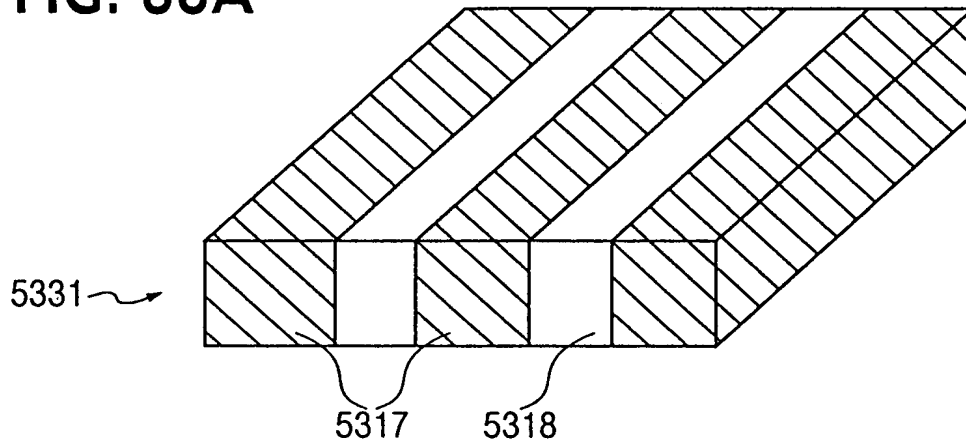


FIG. 88B

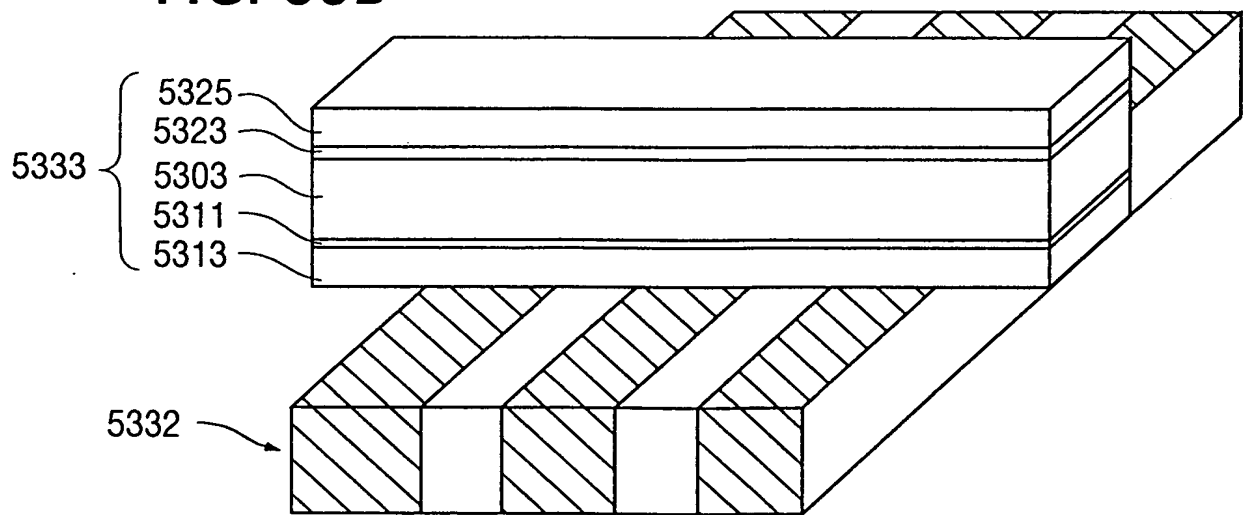




FIG. 88C

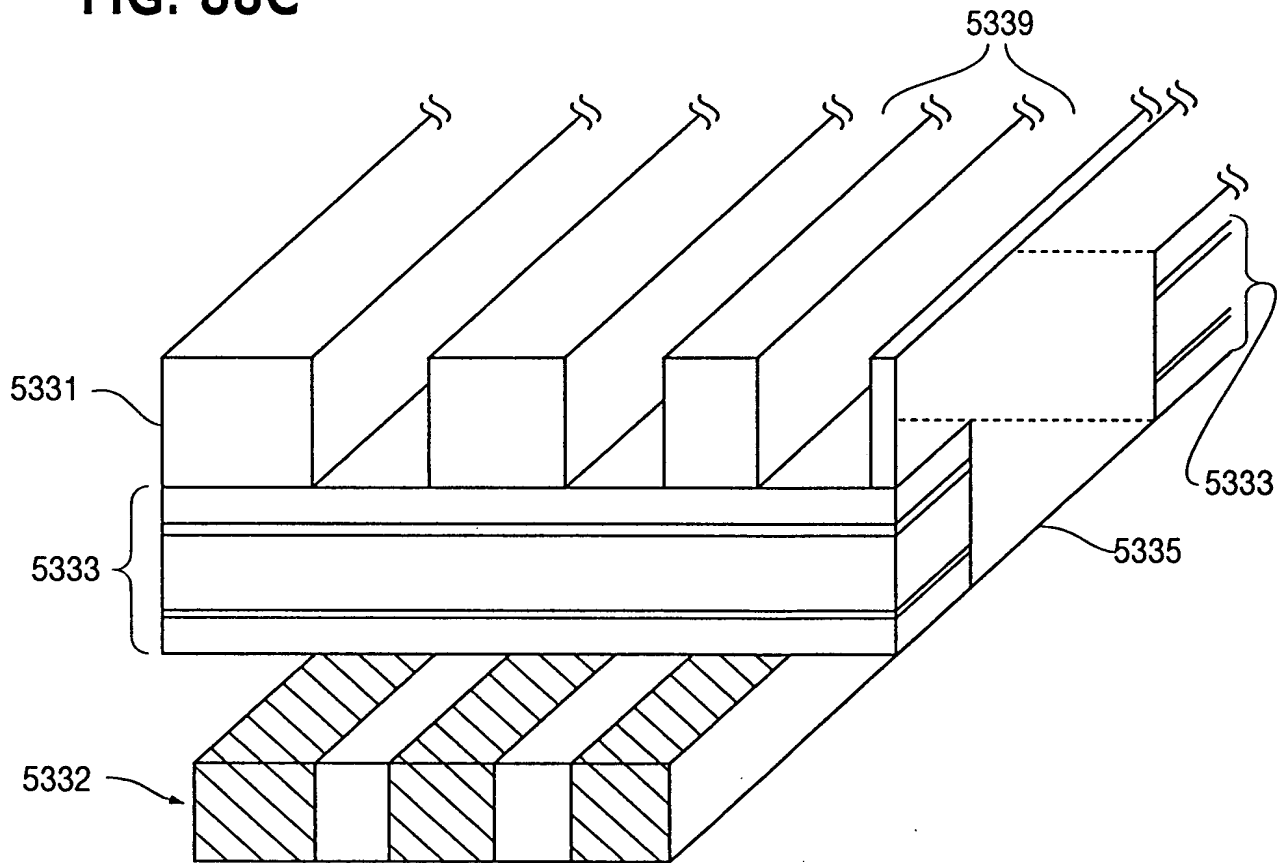




FIG. 88D

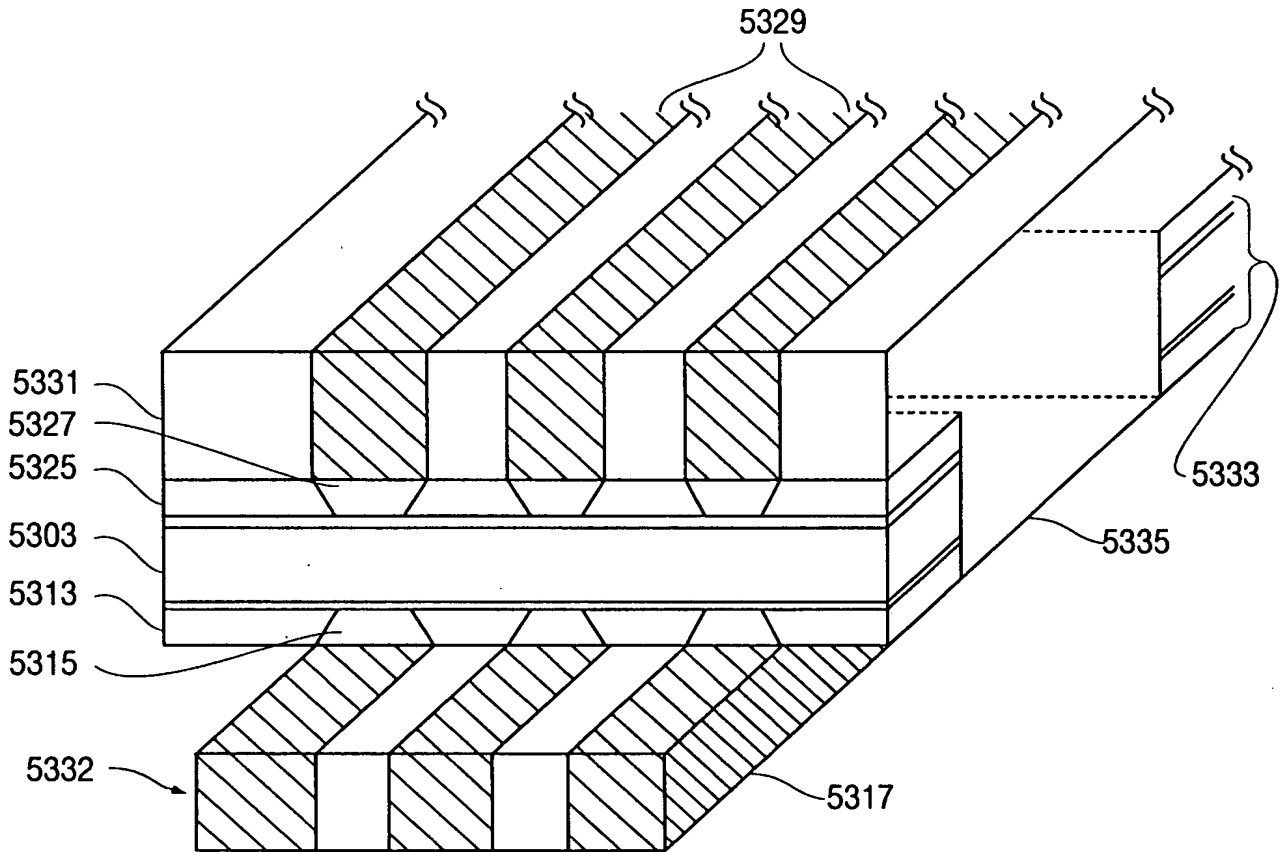




FIG. 89

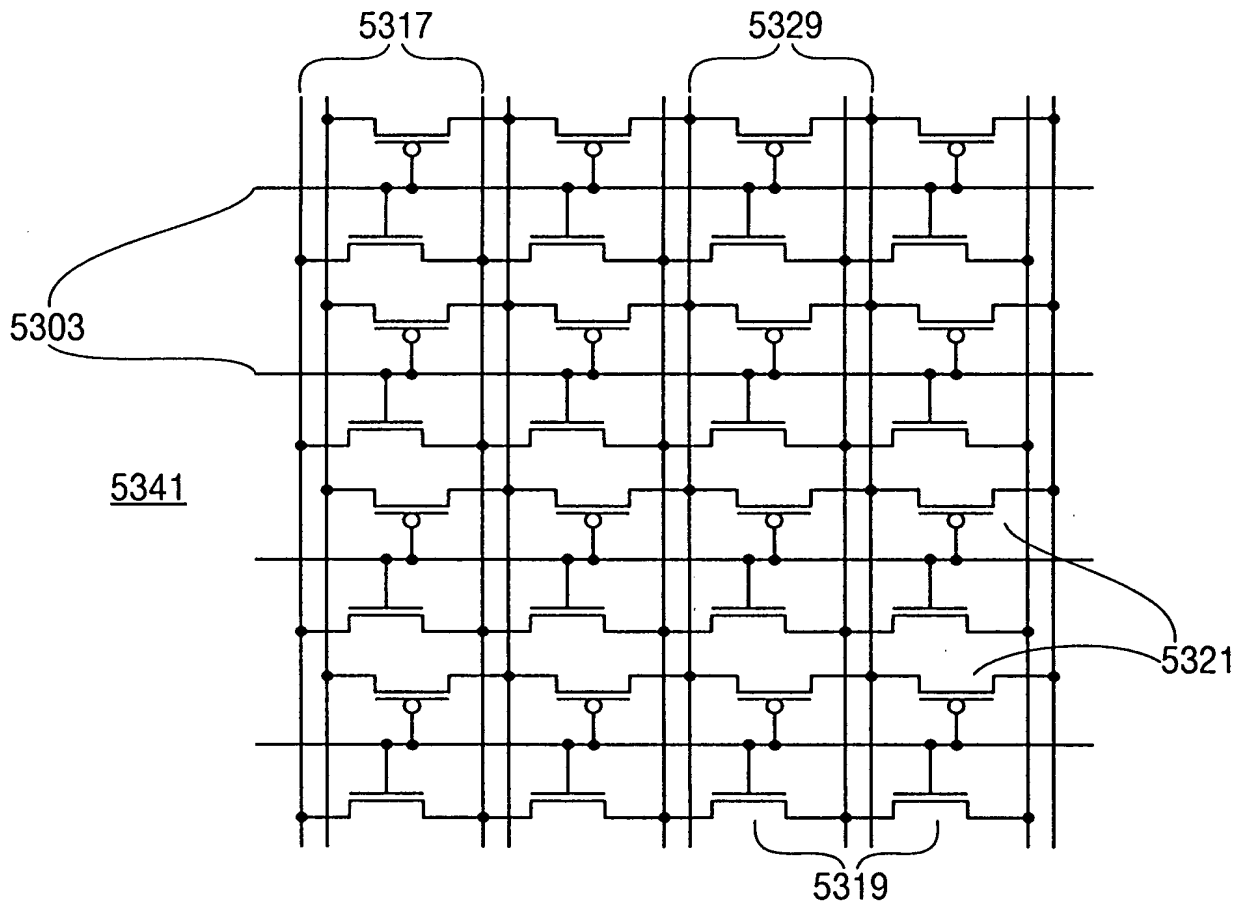


FIG. 90

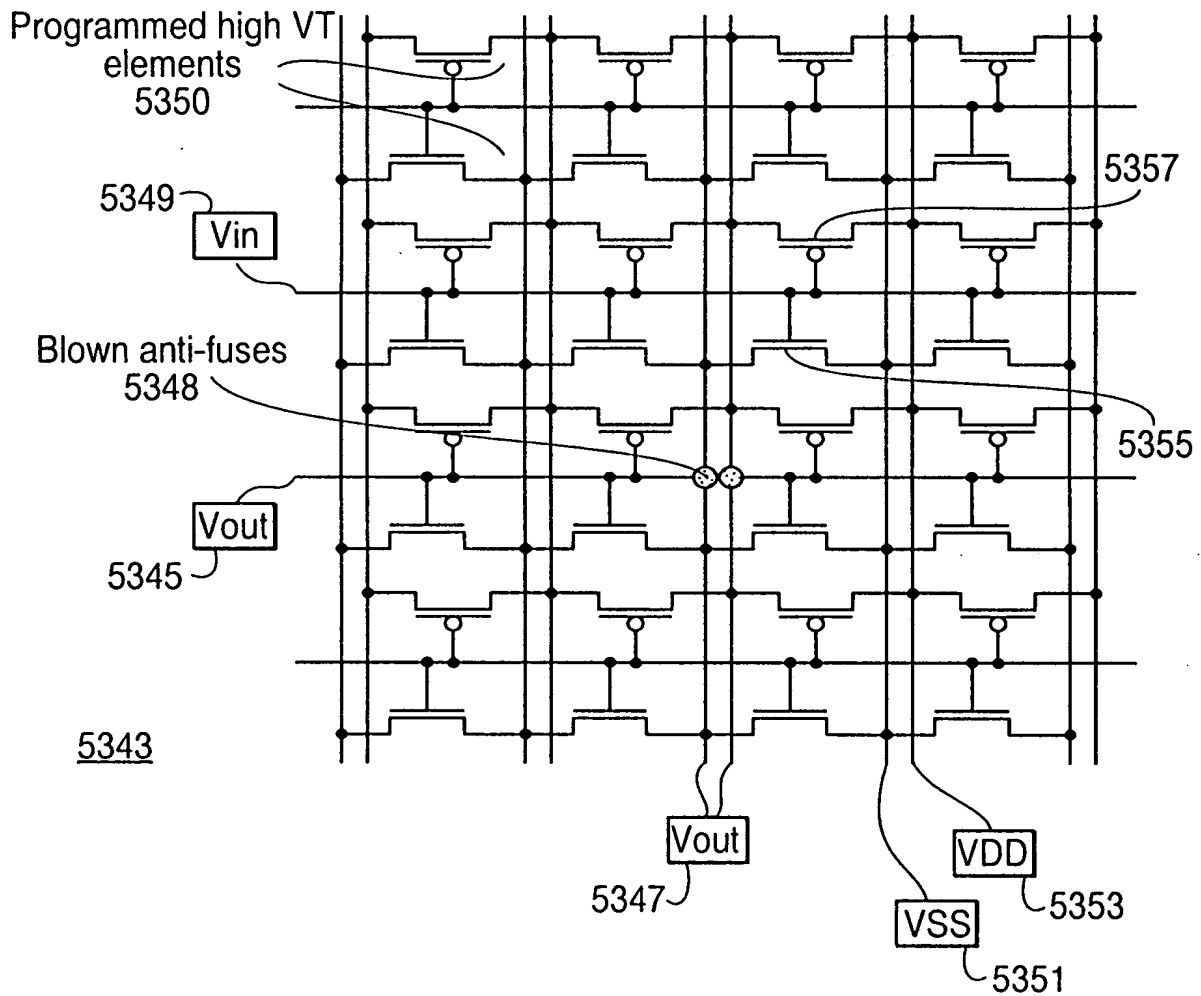




FIG. 91

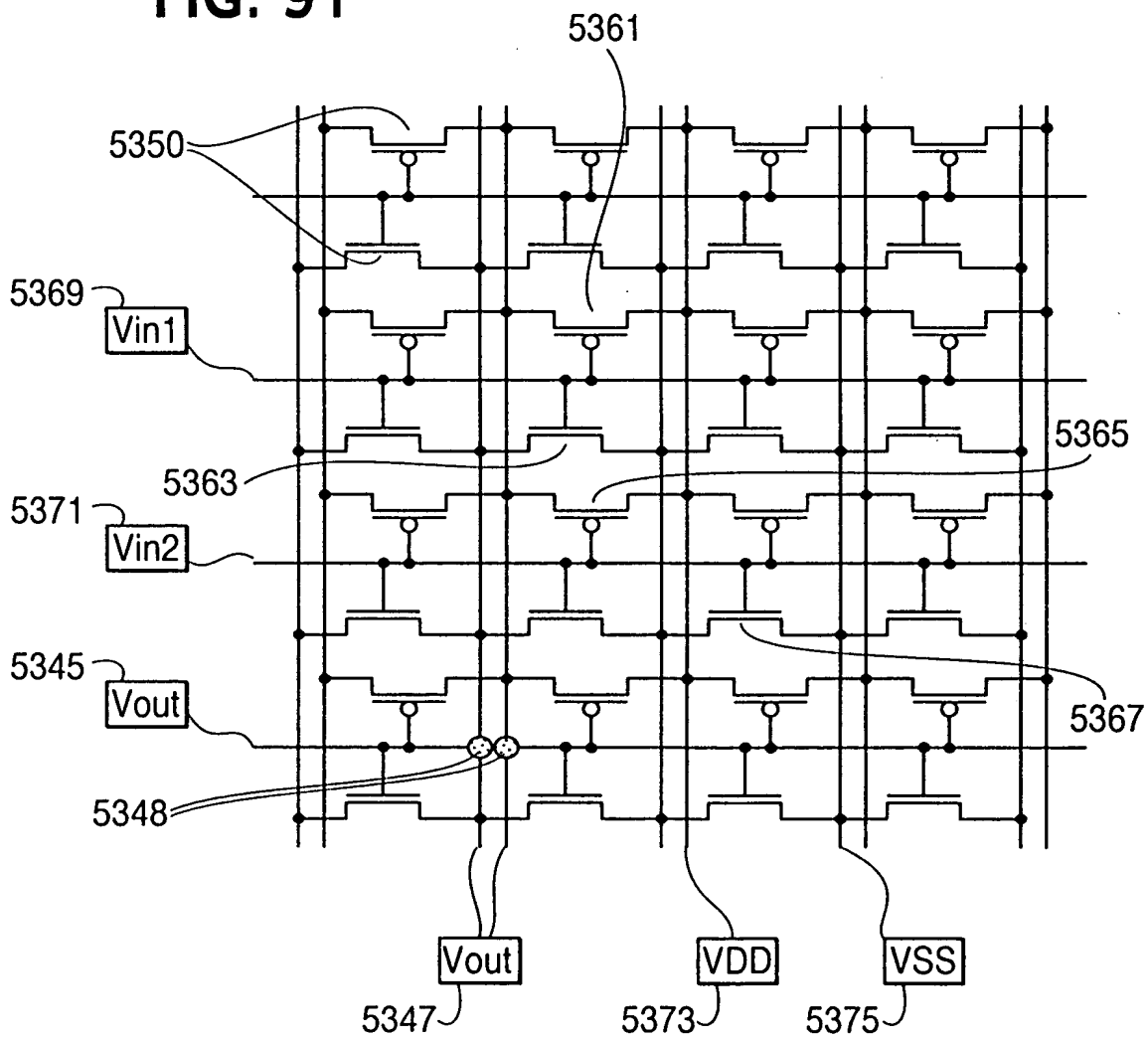


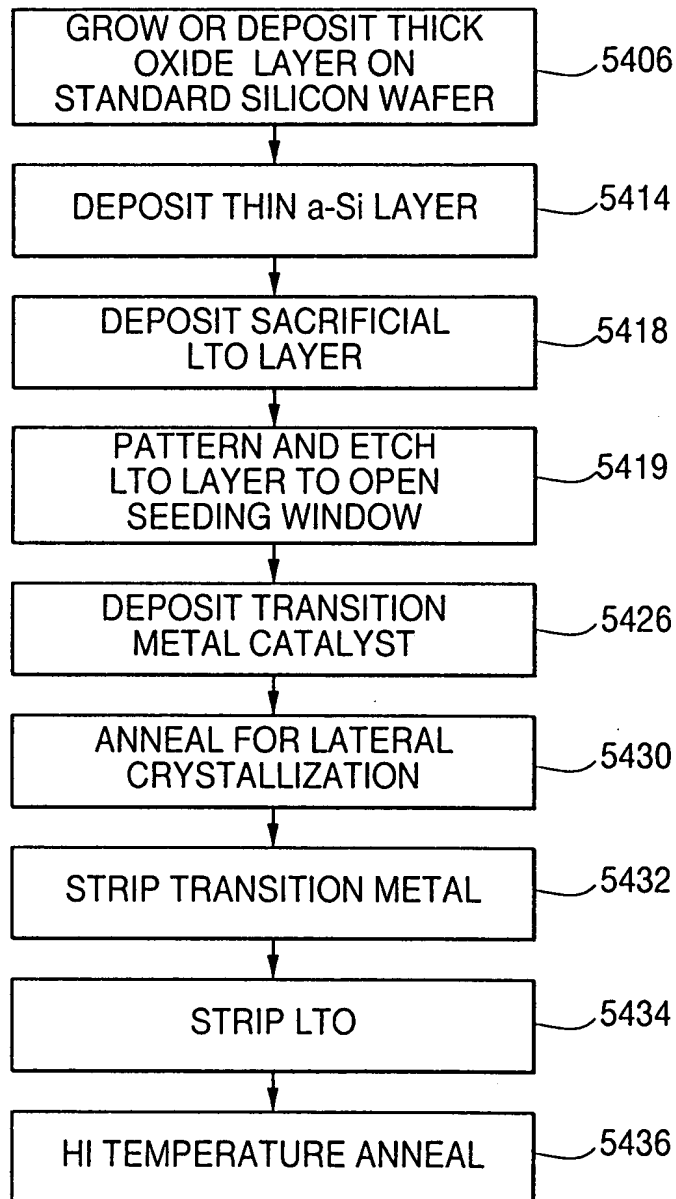
FIG. 92

The diagram illustrates a memory array structure. It features a grid of cross-coupled inverters (latch transistors) and access transistors. The array is organized into rows and columns. The columns are labeled at the bottom as BL (5396), VSS (5398), VDD (5399), and BL-BAR (5397). The rows are labeled on the left as WL (5395). The access transistors (5389, 5390) are connected to the word lines (WL) and bit lines (BL, BL-BAR). The cross-coupled inverters (latch transistors) are connected to the word lines (WL) and bit lines (BL, BL-BAR). The diagram also shows various other components and connections, including 5380, 5381, 5383, 5385, 5386, 5387, 5388, 5391, 5392, 5394, 5395, and 5398.



FIG. 93

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FIG. 94F

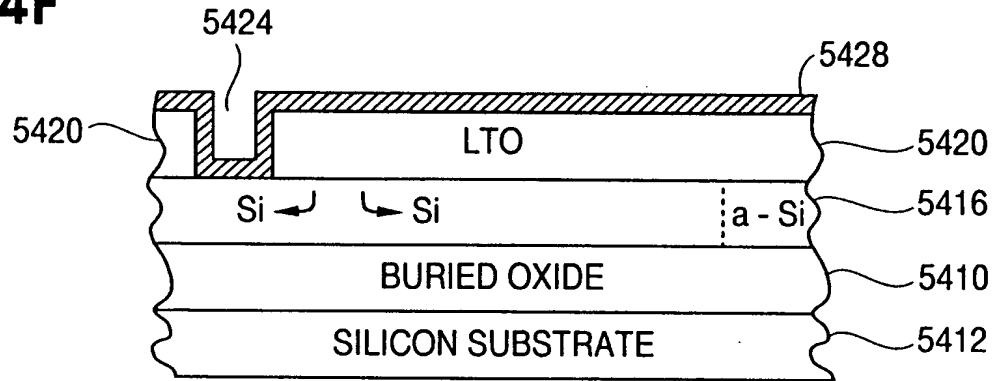


FIG. 94G

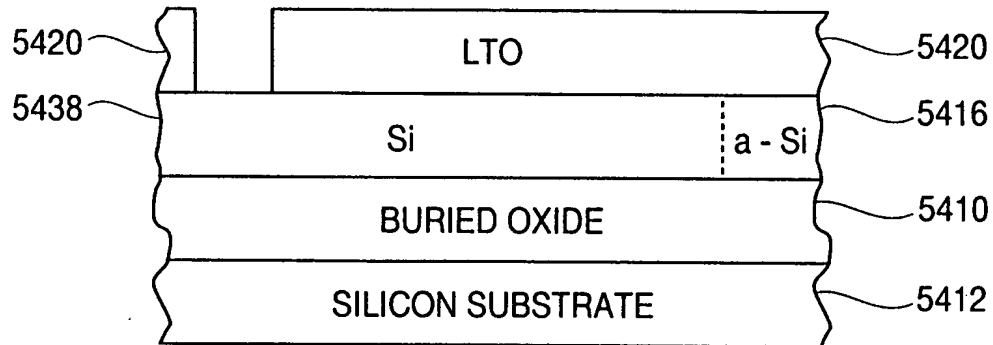
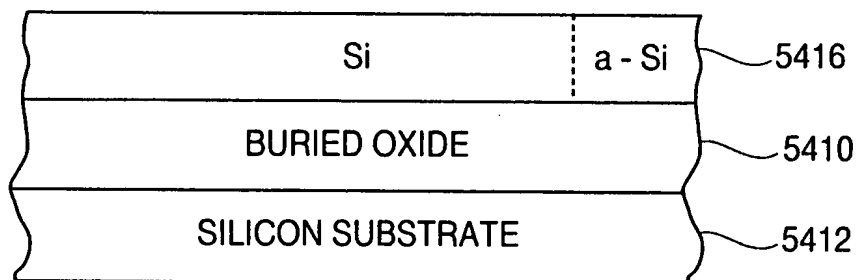


FIG. 94H



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FIG. 95

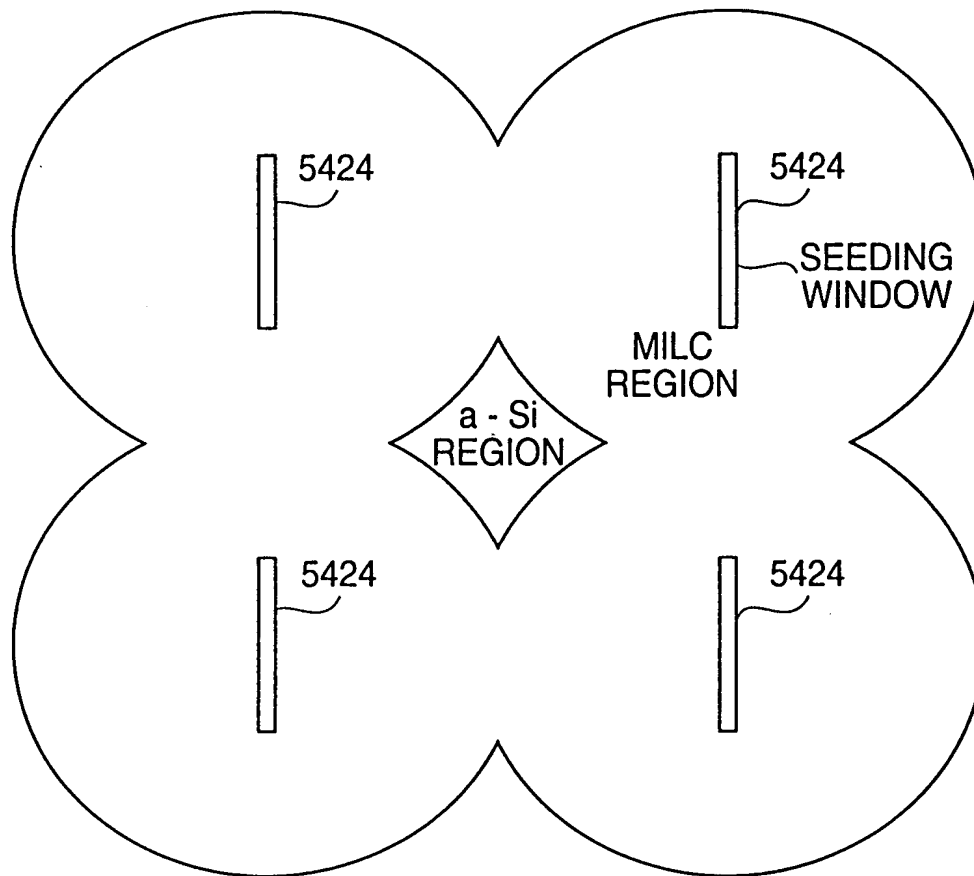


FIG. 95



FIG. 96
(PRIOR ART)

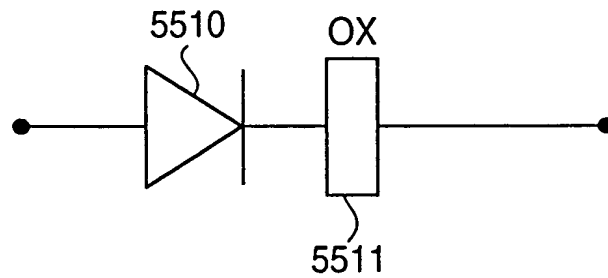
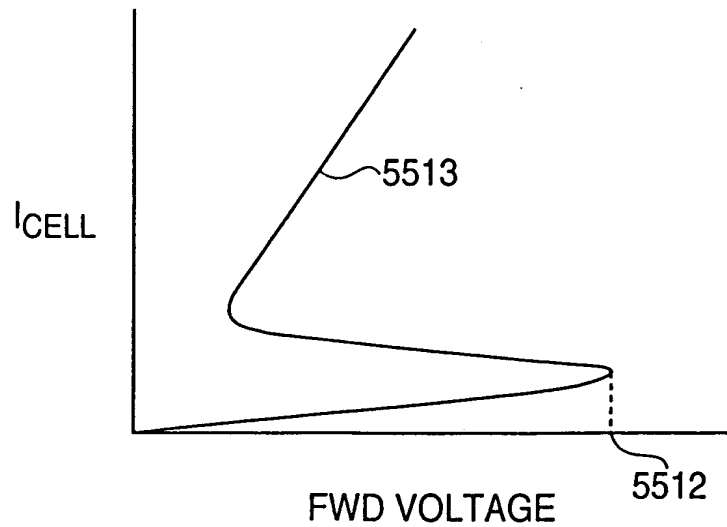


FIG. 97
(PRIOR ART)



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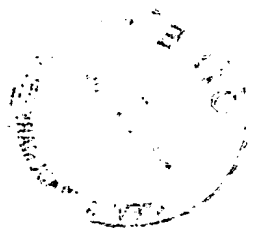
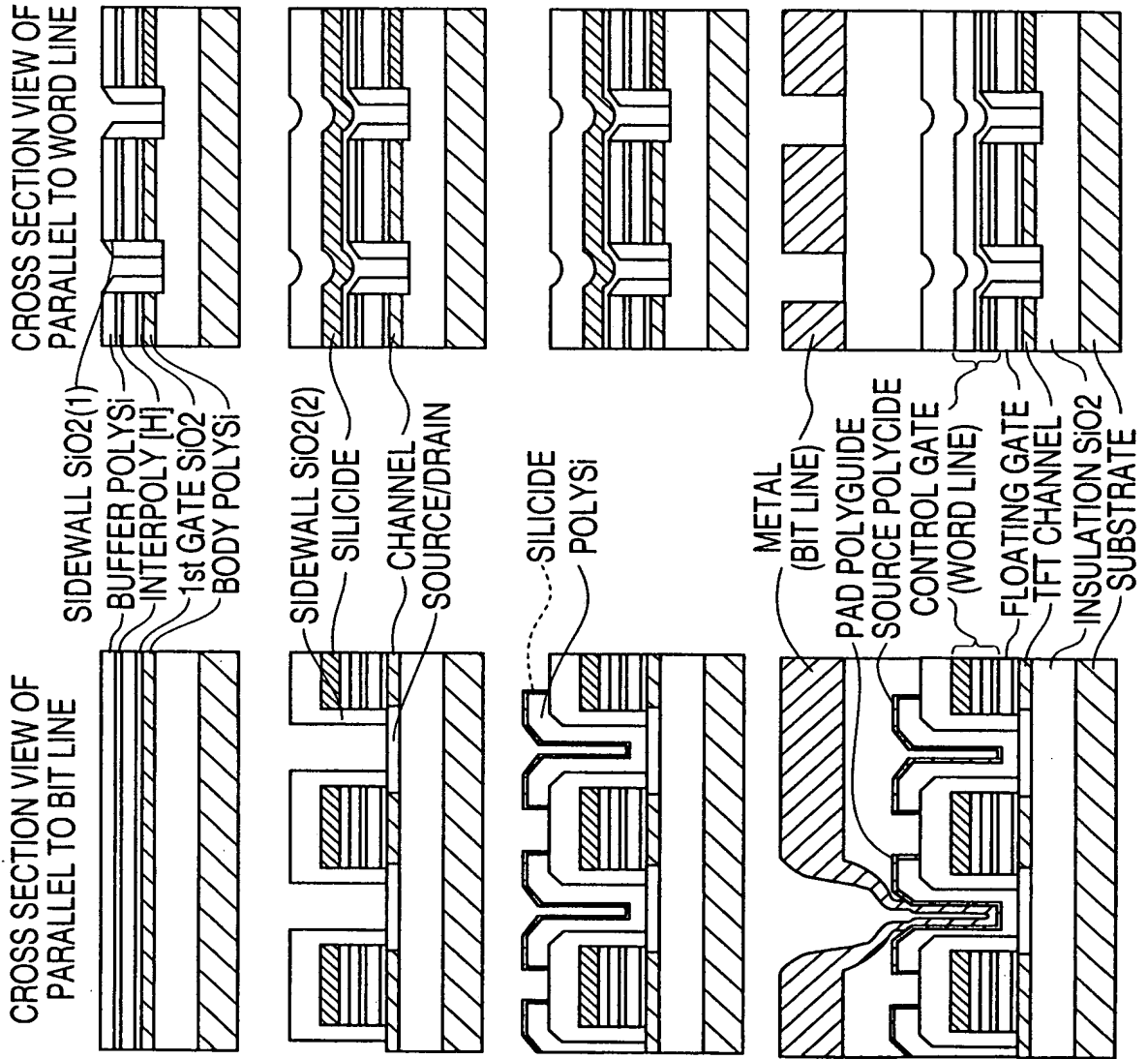
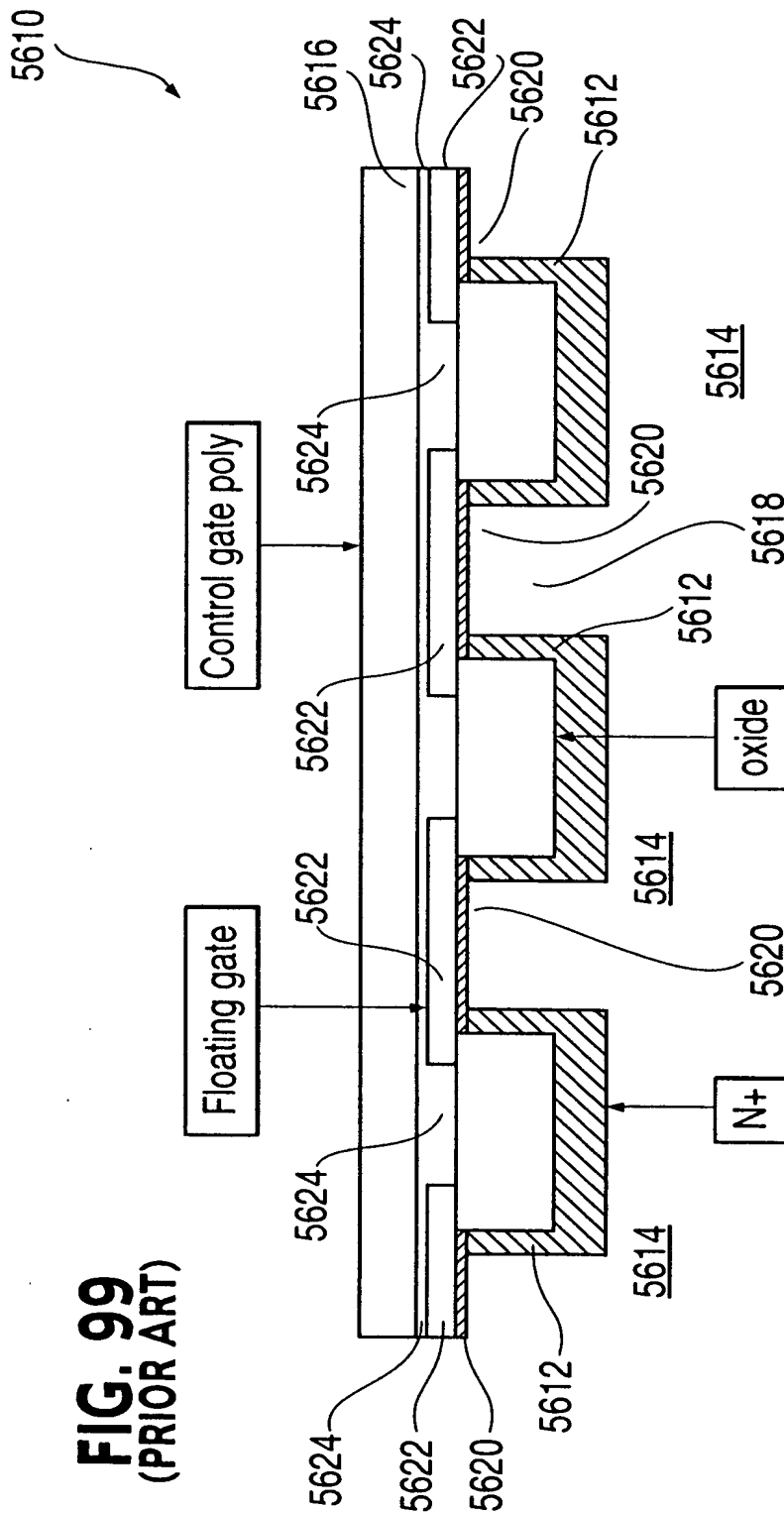


FIG. 98
(PRIOR ART)





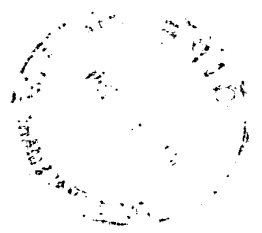


FIG. 100
(PRIOR ART)

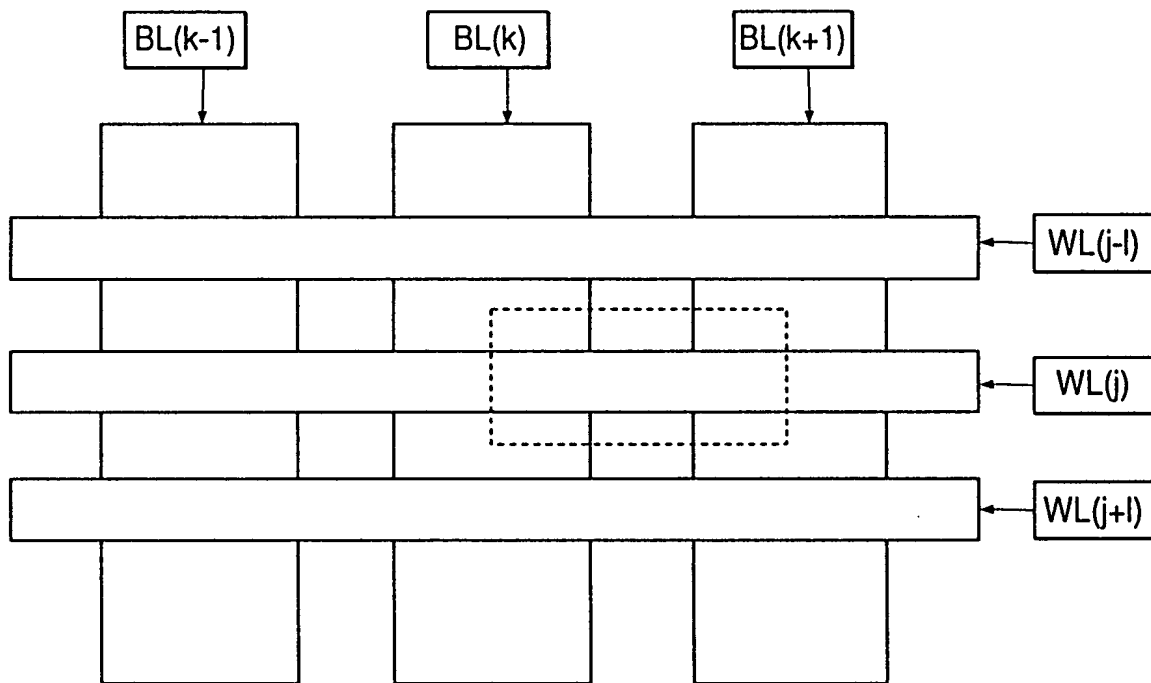




FIG. 101
(PRIOR ART)

